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First demonstration of 300 mm InGaAs-On-Insulator substrates fabricated using the Smart Cut™ technology

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Abstract

This paper reports the first demonstration of 300 mm $In_{0.53}Ga_{0.47}As$-on-insulator substrates. The use of the Smart Cut™ technology leads to the transfer of high quality InGaAs layer on large Si wafer size (300 mm) at low effective cost, considering the reclaim of the III-V on Si donor substrate. The optimization of the three key features of this technology is detailed: 1. The III-V epitaxial growth on 300 mm Si wafer 2. The hydrogen-induced thermal splitting in the epitaxial InP layer 3. The specific direct wafer bonding with alumina oxide.

1. Introduction

$In_{0.53}Ga_{0.47}As$ material is a promising candidate to replace Si in n-channel MOSFETs due to its high electron mobility. In addition, FinFETs or Ultra-Thin Body & Box (UTBB) transistor architectures with high electrostatic integrity are required for the successful introduction of such III-V materials with lower permittivity than Si [1]. InGaAs-OI substrates using direct wafer bonding (DWB) followed by substrate etching, with InGaAs directly grown on bulk InP, have been already demonstrated [2-4]. This expensive process (due to the loss of the InP wafer) is limited to 4'' wafer sizes (maximum InP wafers diameter). Recently, the same technique has been extended to InGaAs layer grown on Si wafer [5-7], solving the wafer size issue but maintaining a significant cost. One paper has reported the use of the Smart Cut™ technology but on a 4'' InP substrate [8].

In this paper, we have successfully fabricated 300 mm InGaAs-OI substrates using the Smart Cu™ technology with III-V layers epitaxially grown on 300 mm Si wafer. We have optimized the III-V epitaxial growth on 300 mm Si wafers, the hydrogen (H^+) implantation inside the InP buffer layer and the specific wafer bonding scheme with alumina oxide layer.

2. 300 mm III-V epitaxial growth

InGaAs-based III-V layers were grown directly on 300 mm on-axis Si(100) substrate by Metal Organic Chemical Vapor Deposition (MOCVD). First of all, native oxide is removed in an in-situ preparation chamber using NF_3/NH_3 plasma. A 510 nm GaAs buffer layer is grown on the Si surface. 154 nm InP buffer layer is then grown for subsequent growth of lattice matched $In_{0.53}Ga_{0.47}As$ layer (from 20 to 54 nm). The crystalline defects are localized in the GaAs layer while no crystalline defects are observed in the thin InGaAs layer, as shown on TEM image in Fig.1. AFM characterization of the 54 nm-thick InGaAs surface reveals a RMS roughness value of 1.57 nm (Fig.2). This value is low considering the large lattice mismatch between Si and InGaAs (about 8 %) and our thin total buffer thickness (= 665 nm). Good thickness uniformity is obtained all across the 300 mm wafer (Fig. 3).

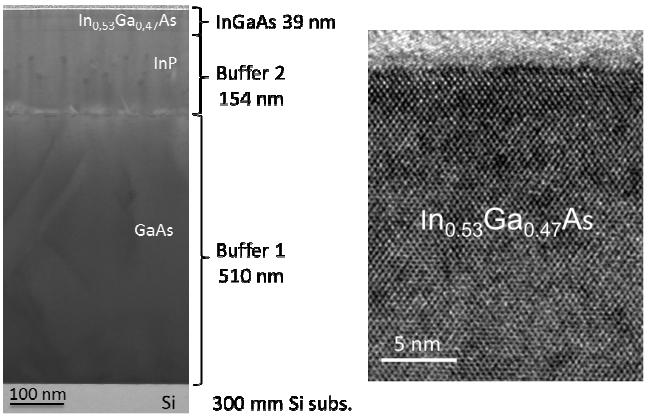

Fig. 1: TEM image of the complete III-V epitaxial stack and HR-TEM on InGaAs channel

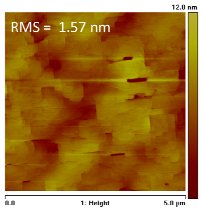

Fig. 2: 5x5 µm² AFM scan of the 54 nm-thick $In_{0.53}Ga_{0.47}As$.

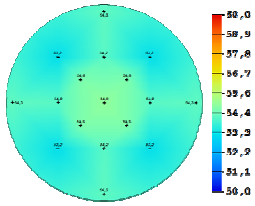

Fig. 3: InGaAs thickness mapping across the 300 mm wafer. Avg. = 54.1 nm. 3σ = 1.7 nm.

3. InGaAs-OI substrate fabrication

The fabrication process of the InGaAs-OI substrates is reported in Fig. 4. A 20 nm-thick Al_2O_3 layer was deposited on the 300 mm III-V epitaxial donor by Atomic Layer Deposition (ALD) at 300°C using Tri-Methyl-Aluminum (TMA) and H_2O as precursors. To avoid the creation of unstable III-V oxides, the starting Al_2O_3 deposition conditions were modified by injecting first TMA pulse after native III-V oxide removal. Next, the Al_2O_3 is capped with a SiO_2 layer (Fig.4a), and annealed at 600°C under N_2 flow to ensure degassing. The H^+ implantation is located inside the 154 nm-thick InP buffer layer. DWB is realized on a thermally oxidized Si substrate using a $SiO_2//SiO_2$ bonding after a polishing and cleaning surface preparation (Fig.4c). The splitting is performed by thermal annealing at 350°C (Fig.4d). 300 mm post splitting III-V-OI are obtained without any bonding defects (Fig.5). TEM image (Fig. 6) confirms the good crystallinity of the transferred InGaAs layer. The remaining InP layer is wet-etched in hydrochloric solution to expose the InGaAs channel. X-ray diffraction analysis (Fig. 7) reveals high quality of the transferred layer It is found that the Full Width at Half Maximum (FWHM) of the corresponding rocking curve around (004) InGaAs reflection is 1370 arcsec. This value corresponds to a low threading dislocation density (TDD) of about 3.10^9 cm^{-2} according to Ayer's model [9].

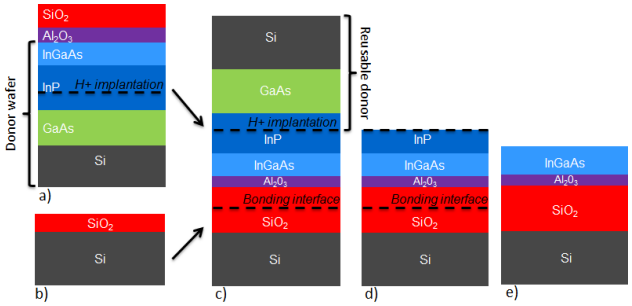

Fig. 4 Fabrication process flow of the InGaAs-OI wafers using the Smart Cut™ technology.

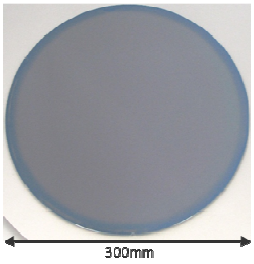

Fig. 5: Picture of the InGaAs-OI after layer transfer

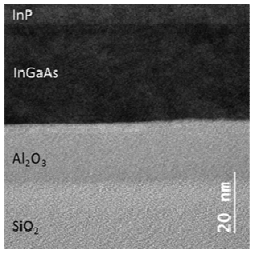

Fig. 6: TEM of the InGaAs-OI after layer transfer.

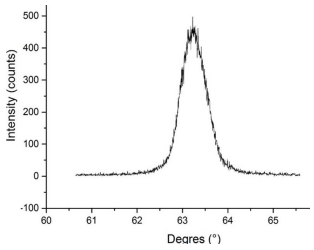

Fig. 7: HR-XRD ω-2θ scan of the final InGaAs-OI layer.

4. Fracture in the InP buffer layer

As far as we know, this is the first demonstration of fracture in an epitaxial InP layer. For bulk InP, implantation temperature was identified to play an important role [10]: some groups reported that the temperature of InP wafer during implantation should be kept below 0°C [11-12], and others claimed that heating the wafers during implantation is mandatory [12-13].

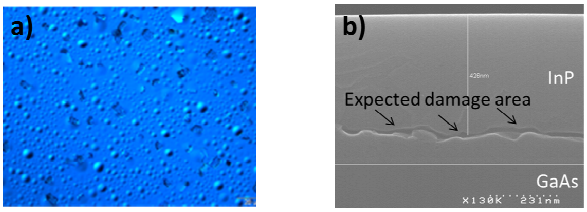

Fig. 8: a) Optical microscope images of the InP surface after H^+ implantation and 300°C annealing b) corresponding SEM image

We performed H^+ implantations in the InP epitaxial buffer layer at different temperature using 300 mm Al_2O_3/InP/GaAs/Si wafers. In our case, we were able to obtain fracture using "standard" temperature control during implantation, i.e the wafers were maintained close to room temperature (RT) thanks to a backside gas cooling combined with water circulation in the chuck. Optical microscope observations showed that we are able to obtain blisters and local exfoliated areas after a 300°C annealing (Fig 8a). It corresponds to micro-cracks localized in the InP layer, as observed in cross-section SEM images (Fig.8b). These results indicate the layer transfer capability, which has been confirmed during the InGaAs-OI fabrication.

5. Bonding condition optimization

The bonding interface quality of different bonding configurations (Al_2O_3//Al_2O_3, Al_2O_3//Si, Al_2O_3//SiO_2, and Al_2O_3/SiO_2//SiO_2) were studied as a function of post bonding annealing. Silicon substrates were used for this study and Scanning Acoustic Microscopy (SAM) images of the results are presented in Fig.9. Al_2O_3 were pre-annealed at 600°C in N_2 ambient and then cleaned in megasonic de-ionized water before bonding. SiO_2 were prepared by polishing and hydrophilic cleaning. At RT, no defects were observed after bonding for all stacks thanks to these efficient cleaning processes (Fig.9). Increasing the post bonding annealing temperature, only the Al_2O_3/SiO_2//SiO_2 bonding presents a good interface quality until 600°C. This configuration avoids the diffusion of bonding interface water at the Al_2O_3/Si interfaces, which are known to be weak and easily defectives [14-15].

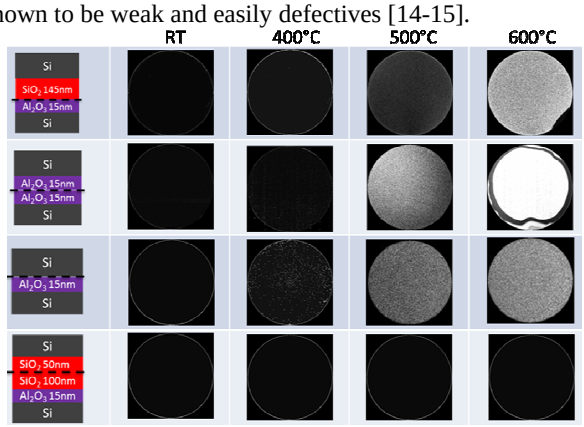

Fig. 9: SAM images of the bonding interface quality for different bonding configurations vs post bonding annealing

6. Conclusions

We demonstrated the successful fabrication of 300 mm InGaAs-OI substrates from direct growth of InGaAs on Si substrate and using the Smart Cut™ technology. Key process elements have been detailed and this work can serve as a ground for future 300 mm InGaAs-OI substrate developments.

Acknowledgements

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