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High Mobility N-MOSFETs on GeSn Film Formed By Solid Phase Epitaxy with Surface Passivation by Oxygen Plasma Treatment

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I. Introduction

As VLSI technology goes beyond 11 nm node, it necessitates novel materials to replace conventional Si to empower aggressively scaling for CMOS devices. Among the promising materials, Ge holds the great potential to fuel the performance enhancement for CMOS devices due to its superior electron and hole mobility to Si counterpart. Recently, GeSn has demonstrated the capability to further improve drive current for P-MOSFETs because of even higher carrier mobility [1]. On the other hand, although higher electron injection velocity than Ge has been confirmed by simulation [2], GeSn N-MOSFETs have been rarely reported in the literature [2] and the device performance still has room to improve. Currently all the reported GeSn N-MOSFETs were fabricated on epitaxial GeSn film grown by MBE [3] or CVD [1, 2] which require rigorous control of process parameters. In addition, to achieve desirable interfacial quality between gate dielectric and GeSn, many surface passivation approaches such NH_4S [4], SiH_6 [5], Ge capping layer/GeO_x [2, 6], and $GeSnO_x$ [7] have been explored. For GeSn N-MOSFETs, the latter three approaches were investigated. Although passivation by SiH_6 [5] is promising, the quantification of interfacial quality and carrier mobility were not well studied. Ge capping layer/GeO_x [2, 6] improves device characteristics, however, I_{ON}/I_{OFF} ratio and mobility need further improvement. $GeSnO_x$ passivation layer can be formed prior to high-κ dielectric deposition by rapid thermal oxidation (RTO) of GeSn surface [7]. It indeed paves a good avenue to implement high-performance GeSn N-MOSFETs, nevertheless, the process may complicate the process since switching between RTO tool for surface passivation and subsequent atomic layer deposition (ALD) tool for high-κ dielectric is unavoidable.

Aiming at the aforementioned process limits, GeSn N-MOSFETs fabricated on GeSn (Sn~4.5 %) formed by solid phase epitaxy (SPE) with $GeSnO_x$ passivation layer grown by O_2 plasma were investigated in this work. The major advances compared to prior arts lie in two aspects. (1) epitaxial GeSn film by SPE [8] has drawn intense interest due to relatively simple process with lower cost. However, only P-MOSFETs [9] were reported on GeSn film by SPE. This is the first demonstration showing that SPE is also an eligible technique to empower high-performance GeSn N-MOSFETs. (2) O_2 plasma for $GeSnO_x$ passivation layer growth can be integrated into the same ALD tool for high-κ dielectric deposition, making the process simpler. More importantly, besides the cost-effective process to implement GeSn N-MOSFETs, the devices exhibit high peak electron mobility exceeding 500 cm^2/Vs which outperforms the data reported in the literature [2, 6] and can be ascribed to high quality of the epitaxial GeSn film as well as the effective surface passivation.

II. Experiment

25-nm GeSn (Sn~4.5 %) film grown on Ge substrate by SPE through amorphous GeSn film deposition and subsequent annealing [8] was used as the channel material for GeSn N-MOSFETs fabrication. After wet cleaning of GeSn surface, O_2 plasma treatment for 60 sec was carried out to form $GeSnO_x$ surface passivation layer. Then 20-nm Al_2O_3 was deposited as the gate dielectric. Note that the passivation layer and the gate dielectric were formed in the same ALD tool at 250 °C without breaking vacuum. Next, the source/drain region was formed by phosphorus (P) implantation with 400 °C or 500 °C annealing in N_2 to activate the dopant. Finally, the N-MOSFETs were completed by depositing and patterning of TaN as the electrode. Brief process flow and device structure are shown in **Fig. 1**.

III. Results and Discussion

Fig. 2 displays the I_D-V_{GS} characteristics for N-MOSFETs with 400 °C and 500 °C activation temperature with drain biased at 0.5 V and 0.05 V. Devices with 500 °C activation reveal higher drive current with large I_{ON}/I_{OFF} ratio more than 4 orders and steeper subthreshold swing (SS) of 156 mV/dec. The higher drive current at 500 °C activation may be directly inferred from higher extent of dopant activation that makes lower source/drain series resistance. However, the lower series resistance cannot well explain the better SS and therefore capacitance-voltage (C-V) curves for N-MOSFETs with different activation temperatures was measured at 1 MHz as shown in **Fig. 3**. From the curves, EOT of 10.0 nm and 9.5 nm are respectively extracted for 400 °C and 500 °C annealed devices. The lower EOT at higher annealing temperature can be ascribed to more densified $GeSnO_x$ and Al_2O_3 that result in thinner thickness or higher dielectric constant. Shown in **Fig. 4** are the C-V curves measured at various frequencies for 500 °C annealed devices and the slight dispersion in the depletion regime implies good interfacial quality which can be quantified by the interface trap density (D_{it}) obtained by conductance-voltage (G-V) characteristic (not shown). From the peak value of G-V, the D_{it} values for 400 °C and 500 °C annealed devices are 7.5×10^{11} $cm^{-2}eV^{-1}$ and 1.64×10^{11} $cm^{-2}eV^{-1}$, respectively. The low D_{it} value implies that $GeSnO_x$ grown by O_2 plasma can effectively passivate the GeSn surface dangling bonds. **Fig. 5** shows the C-V hysteresis at various frequencies defined by the amount of flatband voltage shift from ±3 V bi-directional voltage sweep. Devices with 500 °C activation show smaller hysteresis which is less than 90 mV and it indicates that the amount of bulk traps in the dielectric is limited. Since devices with 500 °C activation correspond to higher capacitance and lower D_{it}, it well explains why steeper SS can be achieved. Note that the SS is not as good as those reported in the literature, it is primarily due to the large EOT arising from the thick Al_2O_3 and an even steeper SS is highly expected by shrinking the EOT. From the C-V characterization, it suggests that the activation temperature not only determines source/drain resistance, it also plays an essential role in controlling the interface and bulk dielectric quality. Shown in **Fig. 6** are the electron mobility as a function of inversion electron density for devices with different activation temperatures. Devices with 500 °C activation reveal higher mobility and can be attributed to the lower D_{it} and fewer bulk traps that make less undesirable carrier scattering. Note that a peak electron mobility of 518 cm^2/Vs is obtained for 500 °C annealed devices and the value also outperforms other GeSn-based N-MOSFETs [2, 6]. This high peak mobility attests to the high quality of the interfacial condition, bulk dielectric as well as the epitaxial GeSn film. **Fig. 7** shows the impact of gate electrical stress time on threshold voltage (V_T) and SS for 500 °C activated N-MOSFETs where an effective electric field of 11 MV/cm

is applied on the gate electrode as the electrical stress. Desirable reliability in terms of SS degradation less than 5 % and V_T shift smaller than 10 mV are achieved even the stress time prolongs to 1000 sec and it implies that the gate dielectric quality is robust enough against the rigorous stress condition. **Table I** summarizes the major device parameters for GeSn N-MOSFETs reported in the literature.

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IV. Conclusion

Epitaxial GeSn film formed by SPE was explored as the channel material for N-MOSFETs in this work. Gated by $GeSnO_x$ passivation layer grown by O_2 plasma and Al_2O_3 dielectric, the devices with 500 °C activation demonstrate exceptional competence to be applied to next-generation GeSn technology in terms of high I_{ON}/I_{OFF} ratio of more than 4 orders, desirable SS of 156 mV/dec, low D_{it} of 1.64×10^{11} $cm^{-2}eV^{-1}$ and most importantly, high peak electron mobility of 518 cm^2/Vs.

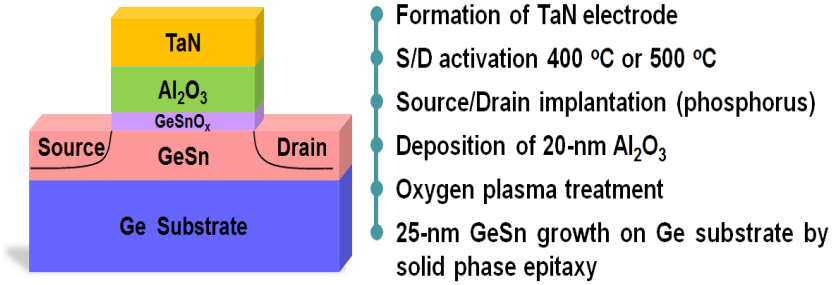

Fig.1 Device structure of GeSn N-MOSFETs and the corresponding process flow where the GeSn was formed by solid phase epitaxy.

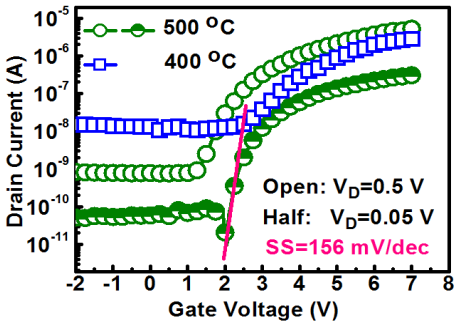

Fig. 2 I_D-V_{GS} curves for 400 °C and 500 °C activated devices with drain biased at 0.5 V and 0.05 V.

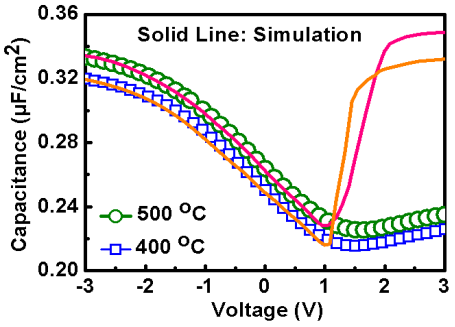

Fig. 3 EOT extraction for devices with different activation temperature.

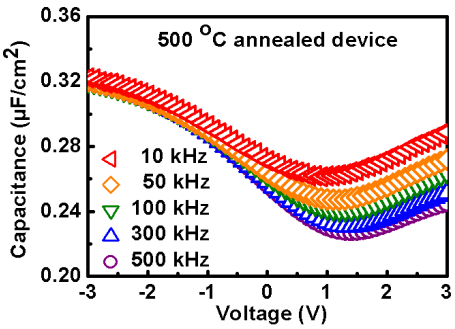

Fig. 4 C-V Frequency dispersion for 500 °C activated devices.

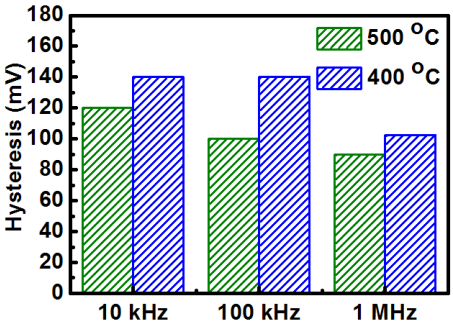

Fig. 5 Frequency-dependent C-V hysteresis for different activation temperature.

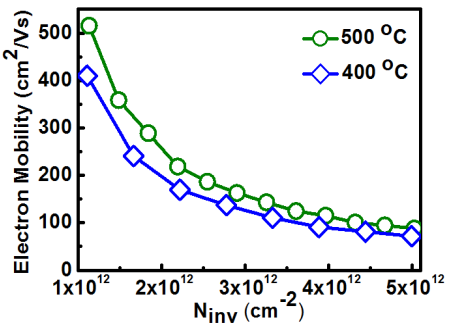

Fig. 6 Electron mobility vs. inversion charge for 400 °C and 500 °C activated devices.

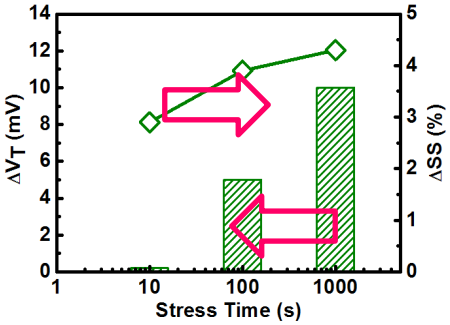

Fig. 7 Time evolution of ΔVt and ΔSS under the stress field of -11 MV/cm.

Reference	2012 Ref [2]	2013 Ref [5]	2012 Ref [6]	2012 Ref [7]	This work
Sn %	5.0 %	2.4 %	6.0 %	2.4 %	4.5 %
Gate Length (μm)	50	6.5	5	6.5	20
Surface Passivation	Ge	Si	2-nm Ge/GeO_x	$GeSnO_x$	$GeSnO_x$
Gate Dielectric	8 nm ALD Al_2O_3	5.4 nm ALD HfO_2	ALD Al_2O_3	6 nm ALD Al_2O_3	20 nm ALD Al_2O_3
I_{ON}/I_{OFF} Ratio (order)	~2.2	~3.3	~4	~3.5	~4.1
Peak Mobility (cm^2/Vs)	~240	NA	~325	NA	518
SS (mV/dec)	NA	195	~107	128	156

Table I Comparison of main devices parameters among various GeSn N-MOSFETs reported in the literature.

References

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