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# High Performance Electronics Based on Novel Two Dimensional Materials

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**Abstract**

**As a strong candidate for future electronics, atomically thin novel two dimensional materials beyond graphene has attracted great attention in recent years, most of which focus on the fundamental material synthesis and low field mobility analysis. However, important figures-of-merit for real applications such as current transport at high field and electrical noise still lacking. A thorough understanding on the performance potential and limit of these material are highly desirable. Here, we focus on arrays of $MoS_2$ transistors with short channel lengths down to 100 nm operated at high field at various temperatures. Highest drive current of 800 μA/μm at 20 K have been achieved without device breakdown. We also studied black phosphorus based transistors using atomic layer deposited high-k dielectrics and compared it with the conventional 90 nm thermal $SiO_2$. The device with high-k $HfO_2$ shows great improvement in drain current and subreshold slope.**

## 1. Introduction

Two dimensional materials beyond graphene have generated great interest recently years owing to their exceptional electronic and optoelectronic properties, which would be promising for future ubiquitous electronics and devices based on novel operation principles such as valleytronics. Among them, semiconducting $MoS_2$, a two-dimensional (2D) layered material of Mo atoms sandwiched between two layers of S atoms, has generated considerable interest [1,2]. Unlike graphene, atomically thin $MoS_2$ is a semiconductor with a bandgap from the 1.2 eV of bulk $MoS_2$ to 1.8 eV of monolayer $MoS_2$, with a mobility in the range from 1-500 $cm^2$/Vs. Moreover, large area $MoS_2$ grown by CVD has been developed, making it a suitable candidate for practical electronic device applications, such as thin film logic circuits and amplifiers with high gain. Fundamental studies on the low field transport properties the metal-semiconductor Schottky contact, structural defect induced scattering, as well as low frequencies noises, have been carried out by various groups. However, the overall assessment of technological relevant parameters such as output capability and signal to noise ratio are still lacking, and their limiting factors are yet to be discussed. Previous studies on $MoS_2$ transistors typically yield output current much smaller than the standard silicon transistor. In the process of evaluating the intrinsic electrical properties of $MoS_2$, large uncertainties exist in the presence of significant extrinsic factors such as contacts and gating, and more importantly, the lack of systematic studies on a series of transistors with long-term stability through thermal cycles[3]. Another emerging material is few layer black phosphorus, Recently, black phosphorus (BP) is found to be a layered material with tunable bandgap ranging from ~0.3 to ~2.0 eV. Field-effect transistors (FETs) based on few-layer BP show encouraging results with high hole mobility up to 1000 $cm^2$/V•s and even higher with hexagonal boron nitride as dielectric[4,5]. However, despite the progress made on high-performance BP pFETs by several groups, detailed research on the output performance and limits of BP nFETs is still lacking, which is a key to realize complementary metal-oxide semiconductor (CMOS) and functional circuits. In addition, the potential to operate in ambipolar regions in the BP transistors could make it ideal for CMOS applications which could greatly reduce the process complexity and cost. Moreover, BP transistors, similar to other 2D semiconductors, suffer from high contact resistance (Rc), which plays an important role not only in output current as studied by many, but also in its noise floor, which determines the signal to noise ratio and remains an important target for every technology node in the CMOS roadmap. As a result, it becomes critical to understand the metal-BP contact and its impact on the ambipolar electronic transport and associated noise behavior. The current fluctuation represented by the noise measurement has been studied on two dimensional material such as graphene and $MoS_2$, but there has only been one such study on BP transistors published very recently, which only focused on the pFET operation. As discussed above, it is imperative to understand both electrical performance and transport mechanisms of n-channel and p-channel of BP based devices.

## 2. Results and Discussions

*$MoS_2$ FETs*

$MoS_2$ devices studied here are based on a 90 nm $SiO_2$ back-gated field-effect transistor (FET) configuration. The $MoS_2$ flake was identified and measured by atomic force microscopy (AFM) and the thickness of which is around 6 nm, corresponding to about 9 layers. Arrays of devices with four different channel lengths from 1 μm down to 100 nm were fabricated by electron beam lithography. Figure 1 shows the direct current (DC) output characteristics of a representative 100 nm channel $MoS_2$ FET at 300 and 20 K, with a drain voltage from 0 to 1.5 V and back gate voltage from -45 to 40 V. Evidently, the current saturation becomes

more significant as the temperature decreases, even starting to show the sign of negative differential resistance (NDR) effect which will be discussed in details later. At room temperature, the maximum drain current is 334 μA/μm for this device, which is larger than previous $MoS_2$ devices reported, including top-gated device with optimized interface engineering. When the temperature decreases to 20 K, the drain current of this device further increases by 240% to 800 μA/μm, which is the highest drive current ever reported so far on any $MoS_2$ FETs. Although it is achieved at low temperature, this greatly improved number extends the current carrying capability of thin film $MoS_2$ transistors much closer to that of the silicon standard. More importantly, it shows the vital roles that extrinsic factors such as doping effects and phonon scatterings play in the $MoS_2$ transistors, where further optimization from these aspects can have huge impact on device performance[3].

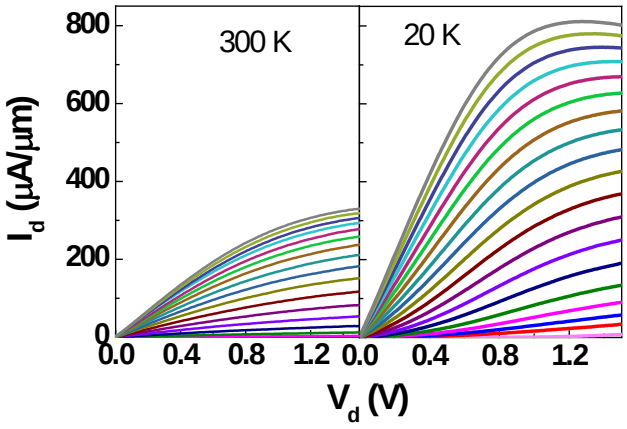


Fig. 1 Transport characteristics of a 100 nm $MoS_2$ FET at 300 K (left) and 20 K (right)[3].

*BP FETs*

In the experiments, the 90 nm $SiO_2$ and 25nm $HfO_2$ are used as gate dielectrics, respectively. The $SiO_2$ was grown by thermal oxidation and $HfO_2$ was grown using a plasma-enhanced atomic layer deposition tool. A p++ Si were used as back gate. The channel lengths range from 100 nm to 2 μm. The source and drain electrodes were fabricated using e-beam lithography and metal evaporation of Ni/Au. The thickness of BP used in this work is 8.6 nm measured by atomic force microscopy (AFM). Figure 2 shows transfer characteristics (Id-Vbg) of the BP device with channel length L= 100 nm at 20 K. The device exhibits clear ambipolar behavior, especially for the one with $HfO_2$ as gate dielectric. Ion/Ioff of more than $10^3$ at $V_{ds}$ = -0.2 V are obtained for BP pFET at 20K. It is obvious that the device with $HfO_2$ shows better ambipolar behavior, as well as steeper subthreshold slope. This is a clear indication that high-k dielectrics has advantages of smaller EOT and as a result, can achieve much better electro-static control by the back gate. Moreover, it can be seen from Fig. 2 that the current level of both p-branch and n-branch is larger for the device with $HfO_2$ than the device with $SiO_2$, which could be attributed to the higher quality interface with the atomic layer deposited $HfO_2$.

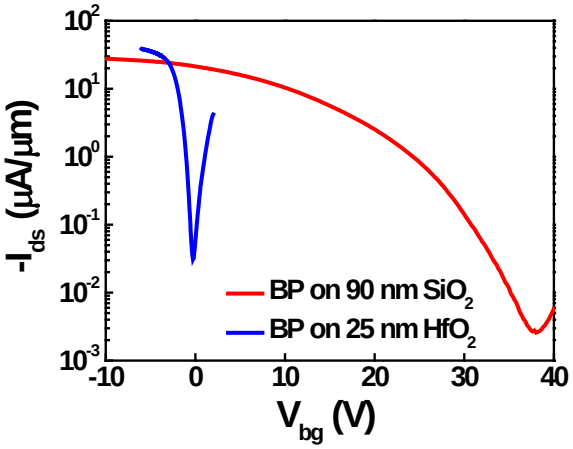


Fig. 2 Transfer characteristics of a 100 nm BP FET at 20 K at $V_{ds}$=-0.2V for two different gate dielectrics.

## 3. Conclusions

High performance 100 nm short channel $MoS_2$ transistors are demonstrated and characterized at 300 K and 20 K. The current of the $MoS_2$ transistor can be significantly increased at lower temperatures due to the improvement of mobility. Highest current of more than 800 μA/μm can be demonstrated for the first time. Black phosphorus based transistor with atomic layer deposited high-k dielectrics are fabricated and compared with the conventional 90 nm thermal oxide. The electrical performance can be greatly improved by the high-k dielectric in terms of subthreshold slope and current.

## References


[1] Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, Nature nanotechnology 6, 147-150 (2011).

[2] Wang, Q. H., Kalantar-Zadeh, K., Kis, A., Coleman, J. N. & Strano, M. S. Nature nanotechnology 7, 699-712 (2012).

[3] X. Li, L. Yang, M. Si, S. Li, M. Huang, P. Ye, Y. Wu, Advanced Materials 2015, 27, 1547.

[4] Li, L. et al. Nat. Nanotechnol. 2014, 9, 372-377.

[5] Liu, H. et al. ACS Nano 2014, 8, 4033-4041.