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Conductive Bridge RAM (CBRAM): functionality, reliability and applications

G. Molas, J. Guy, M. Barci, F. Longnos, G. Palma, E. Vianello, P. Blaise, B. De Salvo, L. Perniola

CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 GRENOBLE Cedex 9, France.
E-mail: gabriel.molas@cea.fr

Abstract

In this paper, we discuss the potentialities of Conductive Bridge RAM (CBRAM) for non-volatile memory applications. By means of experimental studies combined with ab initio calculations and device simulations, we analyze the role of the integrated materials on the memory performances and evaluate the suitability of this memory concept for various applications.

1. Introduction

Conductive Bridge RAM (CBRAM) offer a promising alternative to Flash memories thanks to their low operating voltages, fast switching, scalability and ease of integration in the BEOL of a logic process. They rely on the reversible formation (SET) and dissolution (RESET) of a conductive filament in a resistive layer (electrolyte), this latter being a chalcogenide (GeS_2…) or a metal oxide (SiO_2, high-k material…). The filament results from the dissolution by redox reaction of an active electrode, generally made of Ag or Cu.

2. Results and discussion

In this work, we discuss the functionality and potentialities of chalcogenide (GeS_2/Ag based) and oxide (metal oxide/Cu based) CBRAM (fig.1).

Forming

In the first forming operation, a strong bias has to be applied to create the filament in the resistive layer. This unique step may require specific circuitry to generate higher voltages than what the memory needs to switch in the following cycles. Chalcogenide CBRAM are generally forming free memories, meaning that the initial forming and subsequent SET voltages are equal. In oxide CBRAM, the forming voltage can be reduced by doping the resistive layer [1], creating oxygen vacancies (V_O), and facilitating the Cu injection and filament formation (fig.2).

SET operation

Depending on the applied voltage, various regimes can be distinguished during the operation of chalcogenide CBRAM [2]: at low voltages, filament formation is limited by redox reaction at the interfaces, while at high voltages the drift of Ag+ ions governs the switching speed. It is thus possible to improve the SET speed by tuning the electrolyte (Fig.3) without degrading the disturb performances. In oxide CBRAM, the exponential dependence between the forming time and the applied voltage leads to the time voltage dilemma [3]. Engineering of the resistive layer (fig.4) enables a steeper slope of the characteristics and increases SET speed.

RESET and window margin

The insertion of a bottom interface in both chalcogenide [4] and oxide [5] CBRAM allows to improve the window margin of several decades, thanks to a larger insulating region between the remaining filament and the electrode (fig.5-6). Doping the oxide electrolyte can also result in significant R_{OFF} improvement (fig.7) [1]. Moreover, oxygen vacancy generation is critical in oxide CBRAM to understand the SET and RESET operations (fig.8) [1]. Finally, improving the window margin is generally at the expense of degraded endurance (fig.9), but offers interesting potentialities for high gain CBRAM-based FPGA (fig.10) [6].

Thermal stability

Excellent thermal stability and high temperature retention are required for automotive applications (where stable margin is required at 150°C for ~10-20ys) and secure embedded applications (were the device must sustain soldering reflow of 200-260°C for ~10min). Results reported in the literature so far illustrate the challenge to combine high thermal stability and large window margin (fig.11). The filament dissolution rate during retention strongly depends on the materials. Thus oxide CBRAM offer better thermal stability than chalcogenides, and can show a stable behavior up to 250°C (fig.12) [7]. However, improved retention performances can be achieved with chalcogenide CBRAM by tuning the electrolyte (fig.13) [8]. During retention, the thermal stability is also driven by the programming operations [9]: strong SET current increases the filament thickness and improves LRS stability (fig.14), but tends to degrade HRS retention (fig.15) if insufficient RESET is applied (fig.16). Consequently, a trade-off between temperature range and power consumption should be found.

3. Conclusions

CBRAM offer promising solutions for future non-volatile memory technologies. The proper choice and optimization of the memory stack open the path to various applications.

References

[1] G. Molas et al., 2014 IEDM Tech. Dig., pp.136-139.
[2] F. Longnos et al., proc. of IMW 2013, pp.96-99.
[3] J. Guy et al., 2014 IEDM Tech. Dig., pp.152-155.
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[5] M. Barci et al., proc. of IMW 2015.
[6] E. Vianello et al., 2014 IEDM Tech. Dig., pp144-147.
[7] M. Barci et al., proc. of IRPS 2014, 5E.3.1 - 5E.3.4.
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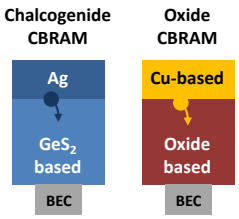

Fig. 1 CBRAM concepts discussed in this work.

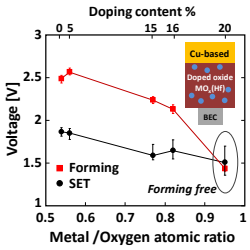

Fig. 2 $V_{forming}$ reduction of oxide-based CBRAM, doping the electrolyte with Hf.

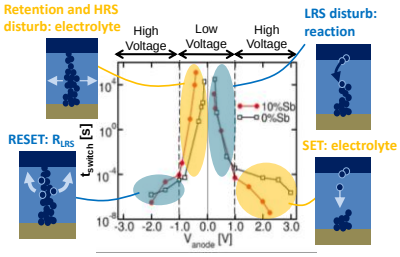

Fig. 3 Switching time for two chalcogenide CBRAM for the various operating regimes. Sb doping of GeS_2 improves SET speed.

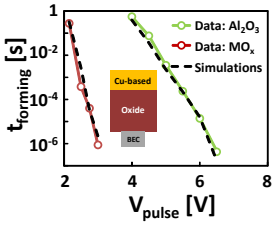

Fig. 4 Forming time/voltage dependence for two oxide based CBRAM.

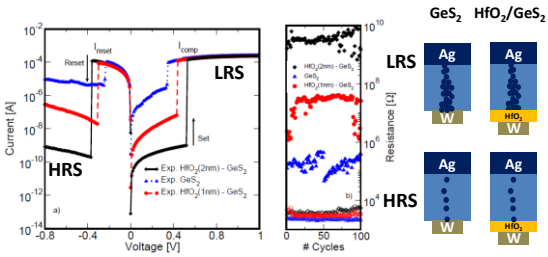

Fig. 5 Switching and cycling characteristics of HfO_2/GeS_2 and GeS_2 CBRAM.

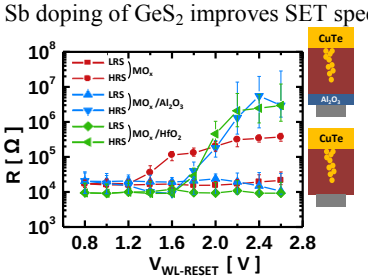

Fig. 6 R_{OFF} improvement with a bottom interface in oxide CBRAM.

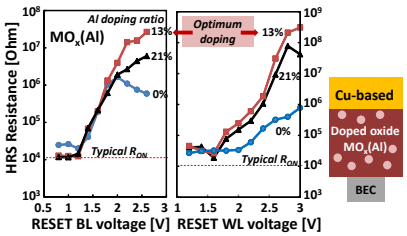

Fig. 7 R_{OFF} improvement with Al electrolyte doping in oxide CBRAM.

	ΔH enthalpy formation (eV)		
Layer	MO_x	MO_x(Hf)	MO_x(Al)
V_O creation	<3.5eV	<3.5eV	<3.5eV
Cu insertion	3.2eV	1.3eV	3.6eV
Cu in V_O	1.3eV	~0eV	-0.2eV

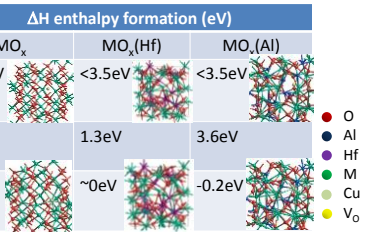

Fig. 8. Calculated formation enthalpy energy using 1st principal calculations for V_O creation, Cu insertion and Cu insertion assuming V_O in various oxide resistive layers.

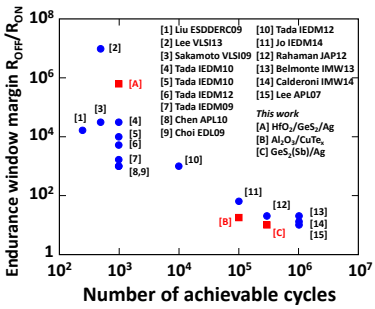

Fig. 9. Window margin as a function of the number of achievable PE cycles for CBRAM reported in the literature.

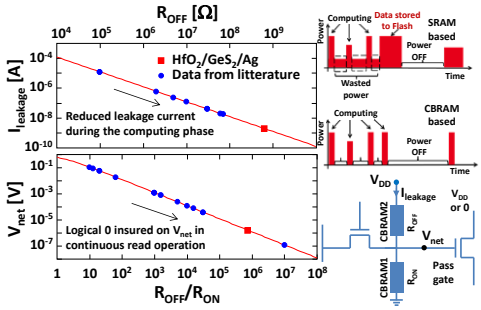

Fig. 10 Low R_{OFF} and high R_{OFF}/R_{ON} allow low leakage current and good efficiency in CBRAM based 1T2R non-volatile voltage divider element for FPGA (V_{DD}=1.2V).

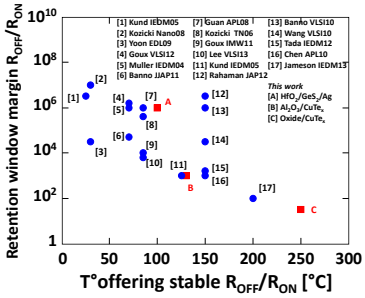

Fig. 11 Reported window margin vs operating T°.

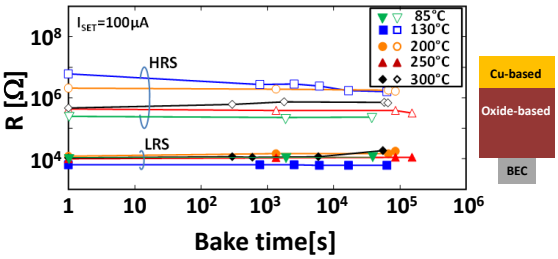

Fig. 12 Retention characteristics of MO_x CBRAM with stable window margin during 10^5s up to 250°C.

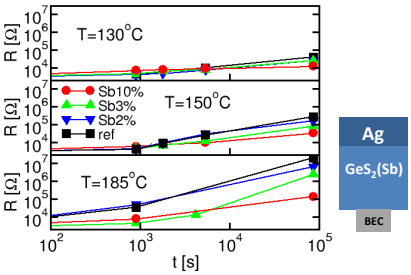

Fig. 13 Retention improvement of chalcogenide CBRAM by Sb doping of GeS_2.

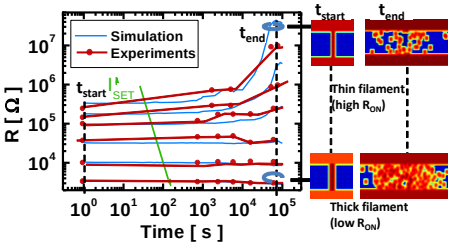

Fig. 14 ON state retention dependence with initial R_{ON} (related to filament thickness)

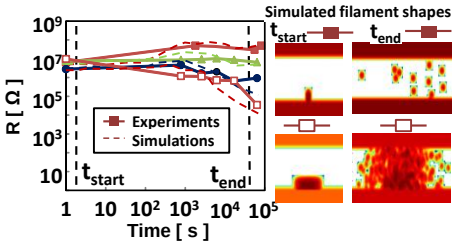

Fig. 15 OFF state retention dependence with previous R_{ON} (related to filament thickness)

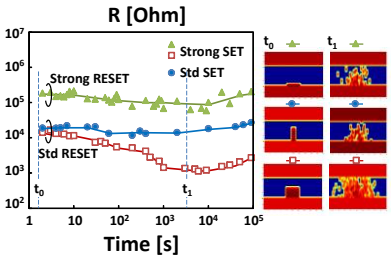

Fig. 16 HRS retention for various initial R_{OFF} (related to insulating gap).