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A 32-kb Embedded SRAM Using 60-nm Crystalline Oxide Semiconductor Transistors and Power Gating with 45-ns 144-fJ/bit Data Backup

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Abstract

A 32-kbit SRAM with backup circuits including C-Axis Aligned Crystalline Oxide Semiconductor (CAAC-OS) transistors (OS-FETs), which have extremely low off-state currents of the order of yoctoamperes, has been prototyped. The backup and the recovery times are 45 ns and 160 ns, respectively. The backup and the recovery energies are 144 fJ/bit and 97 fJ/bit, respectively. By performing power gating (PG), a standby power reduction of 99.9% or more has been demonstrated. Furthermore, we propose power saving technique of selectively using multiple low standby power modes.

1.Introduction

Research in the field of Internet of Things (IoT) has been very active in recent years, and ultra-low-power-consumption devices are required for IoT applications. Because of shrinks and the higher integration in LSIs, leakage power is too large to be ignored. One possible solution is PG, in which power is cut off to blocks of the circuit when they are not in use. However, nonvolatile devices still need to retain data in order to resume computations after PG. There have been previously reported [1–3] on the attempts to reduce power consumption in LSI by employing PG and nonvolatile devices, such as OS-FETs [4–5].

In this study, we prototyped an SRAM with backup circuits including 60-nm OS-FETs (CAAC-OS-based SRAM). We report the time and energy required for the backup and the recovery operations and the standby power reduction due to PG, and propose a novel technique for reducing the power consumption of the embedded memory by introducing multiple low standby power modes.

2. Chip Design and Features

Fig. 1 is a photograph of the prototype 32-kb SRAM chip, and TABLE I lists features of the chip. This prototype chip includes OS-FETs having a channel length scaled down to 60 nm [5]. Please note that the reason of the different sizes of silicon (Si) and OS is simply due to the constraints in our prototype facilities. It should work and improved performance can be expected when we use 60nm for both of Si and OS. An evaluation based on SPICE has been reported in the case where a scaled Si/OS process is assumed [1]. Bitline floating and PG are implemented in order to reduce the standby power. The memory cell array comprised four subarrays, each formed of 128 wordlines × 64 bitlines, and peripheral circuits contains backup and recovery drivers, power switches, and general driver circuits. Figs. 2(a)–(c) show the CAAC-OS-based SRAM cell. Two OS-FETs and two capacitors are added to a conventional six-transistor SRAM cell. The CAAC-OS-based SRAM can replace a conventional SRAM with negligible impact in performance. Furthermore, zero area overhead is achievable because of the stacked Si and OS layers [1].

Power domains are divided into a memory cell array unit (1.8/0 V), a peripheral circuit unit (1.8/0 V), and a backup and recovery driver unit (2.5/−1 V), and each is provided with a power switch (Fig. 3). The OSG lines are controlled by a PG signal, and the power switches are controlled by a PS_PERI signal and a PS_MEM signal. In the chip, the following four low standby power modes are implemented: (1) bitline floating; (2) PG for the peripheral circuit (peripheral PG); (3) PG for the memory cell array (array PG); and (4) PG for all of the domains (all-domain PG).

3. Measurement Results for Power Gating

Fig. 4 shows oscilloscope waveforms of the PG sequence. The backup time of 45 ns and the recovery time of 160 ns are observed. In the recovery sequence, 20 ns is the recovery time excluding the charge time for the power line.

Fig. 5 shows standby power reduction effects for each standby mode implemented in this chip: −3.9% with bitline floating; −0.1% with peripheral PG; −95% with array PG; and <−99.9% with all-domain PG.

For performing PG, overhead energy is consumed in several ways including control of the power switches, the charge of the power line, and the backup and the recovery of data in the memory cells. Therefore, if PG is performed for a period that contains only short power-off time, total power consumption may increase.

Fig. 6 shows power savings with bitline floating and PG as a function of given the idle time (the savings are normalized by the value of the case without bitline floating and PG). When the idle time is shorter than 700 μs, the total power is reduced without performing bitline floating or PG. As shown in Fig. 6, total power is reduced by 1) performing bitline floating when the idle time is 700 μs to 1.55 ms, 2) by performing array PG when the idle time is 1.55 ms to 59.3 ms, and 3) by performing all-domain PG when the idle time is longer than 59.3 ms. It can be expected to reduce the power efficiently by performing these low standby power modes sequentially, even in the application whose waiting time may be randomly distributed.

TABLE II shows comparisons among various PG techniques [1–3]. Our prototype CAAC-OS-based SRAM shows superior frequency for the normal operations and the

backup time and energy. These advantages are obtained by adding a backup circuit to an SRAM cell, which operates very quickly, and by the low-power, fast-write operation of OS-FET memory [5]. The leakage power in our chip was inherently not so high, because the Si technology was 180 nm. The leakage current of a Si-FET becomes larger with miniaturization, and the PG technique becomes more effective. Furthermore, the CAAC-OS-based SRAM is promising for high-frequency applications, which require an SRAM. Although 180-nm Si technology was used in this prototype, higher-frequency operation with miniaturization can be expected [1].

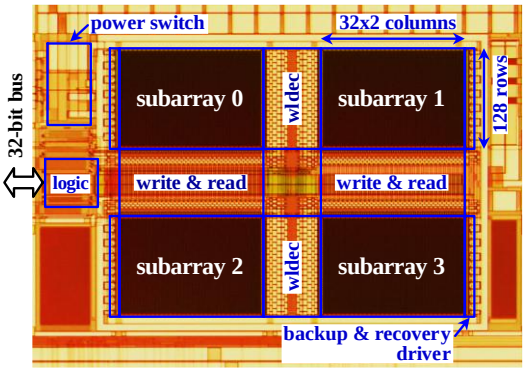

Fig. 1. Chip photograph.

TABLE I. 32-KBIT SRAM FEATURES.

Technology	Si: 180 nm	OS: 60 nm
Organization	1K word × 32 bit = 32 kbit	
Frequency	85 MHz	
Supply voltage	Si: 1.8 V	OS: 2.5/−1 V
Leakage reduction technique	Bitline floating, SRAM cell with a backup circuit, Power switches for array and peripheral circuits	

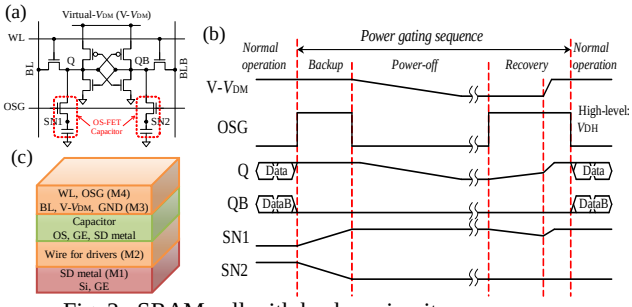

Fig. 2. SRAM cell with backup circuits;
(a) circuit diagram, (b) power gating sequence and (c) layered structure.

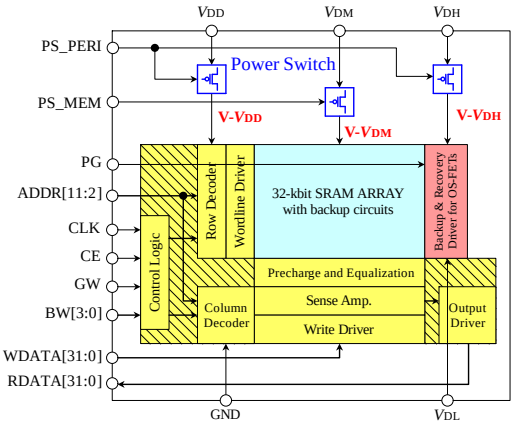

Fig. 3. Power domains in 32-kb SRAM.

4. Conclusion

A 32-kb SRAM chip with backup circuits including CAAC-OS-FETs has been prototyped. By employing PG, the backup time and energy were 45 ns and 144 fJ/bit, respectively, and the recovery time and energy were 160 ns and 97 fJ/bit, respectively.

Standby power reduction effects are obtained for each of the PG modes. We will further develop CAAC-OS technology to achieve lower-power-consumption of memory.

References

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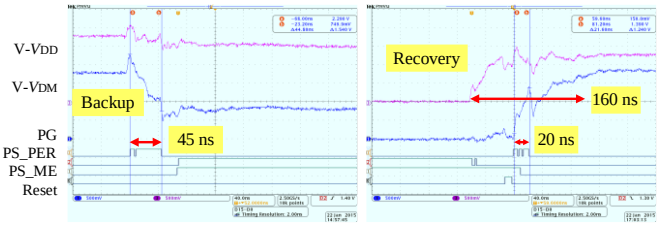

Fig. 4. Oscilloscope waveforms during power gating.

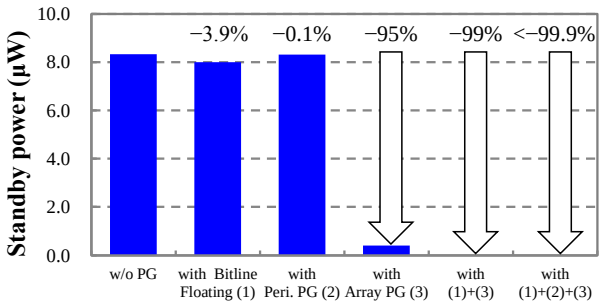

Fig. 5. 32-kb SRAM standby power with low standby power modes.

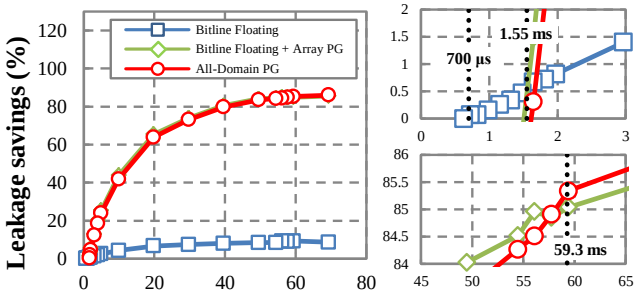

Fig. 6. Leakage savings for various low standby modes as a function of idle time.

TABLE II. COMPARISONS AMONG POWER GATING TECHNIQUES.

	This work	Ishizu [1]	Sakimura [2]	Bartling [3]
NV device	CAAC-OS	CAAC-OS	MTJ	FeCap
Technology	Si: 180 nm OS: 60 nm	Si: 350 nm OS: 180 nm	90 nm	130 nm
Frequency	85 MHz	15 MHz	20 MHz	8 MHz
Supply voltage	Si: 1.8 V OS: 2.5/−1 V	Si: 2.5 V OS: 2.5/−1 V	1.0 V	1.5 V
Backup time	45 ns	80 ns	4 ns*2	320 ns
Recovery time	160 ns*1	400 ns*1	5 ns*2	384 ns*1
Backup Energy	144 fJ/bit	N/A	6 pJ/bit	2.2 pJ/bit
Recovery Energy	97 fJ/bit	N/A	0.3 pJ/bit	0.66 pJ/bit

*1: including charge time for power line.
*2: values from write and read operation of MRAM cell.