

A Study of Array Resistance Distribution and a Novel Operation Algorithm for WO_x ReRAM Memory

K.C. Hsu, F.M. Lee, Y.Y. Lin, E.K. Lai, J.Y. Wu, D.Y. Lee,
M.H. Lee, H.L. Lung, K.Y. Hsieh and C.Y. Lu

Macronix Emerging Central Lab., Macronix International Co., Ltd.

16 Li-Hsin Rd. Hsinchu Science Park, Hsinchu, Taiwan, R.O.C.

TEL: +886-3-5786688 ext 78004, FAX: +886-3-5789087, Email: kerryhsu@mxic.com.tw

Abstract

Resistance distribution of tungsten oxide (WO_x) resistive random access memory (ReRAM) is investigated. Bit-by-bit tracking and bit map comparison show the difficulties in predicting individual cell resistance after each programming operation. Nevertheless, the group behavior follows the Gaussian distribution and is predictable. Based on this finding, a program-verify operation algorithm with constant pulse condition is proposed. This novel new approach not only effectively opens up the memory window but also prevents overstressing in the conventional approach that degrades cell reliability.

A. Introduction

WO_x-based resistive random access memory (ReRAM) is a strong candidate for next generation memory due to its low cost and CMOS compatible process [1,2].

Commonly seen in all types of ReRAM devices, resistance distribution control is a major challenge for sufficient resistance window and affects the product performance including read speed, cycling endurance, and data retention [3,4]. Better resistance distribution may be achieved by high current operation that switches the device harder, but this not only increases the cell size but also causes device degradation resulting in reliability problems.

In this study the resistance distributions of TiN/WO_x/W ReRAM after RESET (resistance switches from low to high) and SET (high to low) operations are carefully inspected and found to be Gaussian. A programming algorithm is then suggested accordingly.

B. Device Structure and Fabrication

A 1 Kbit 1T1R (one transistor with one ReRAM cell) array is used as the test vehicle. Following the standard CMOS FEOL process up to contact W-plug CMP step, WO_x memory layer is formed by modifying a previously reported plasma oxidation process [5] on top of the bit-line contacts in the array area (Fig. 1). Figure 2 shows the detailed device structure and a TEM image. The 3nm-thick WO_x memory layer is sandwiched between TiN and W as the top and bottom electrodes, respectively.

C. Normal Distribution and Random Pattern

The virgin cells are first formed with a forward current pulse through the top electrodes before the normal operations. Figure 3 shows the array resistance distribution after one-shot RESET (forward pulse) or SET (reverse pulse) without further resistance trimming. Although there is slightly overlapping (~ 3%) between high resistance state (HRS) and low resistance state (LRS), the resistance histograms for both HRS and LRS follow the Gaussian function

(Fig. 4). This suggests that both RESET and SET operations are statistical in nature. Figure 5 further shows the resistance distribution tracking in a SET-RESET-SET operation sequence. It is clear that the resistance of any single cell in the array is not predictable but the group resistance always follows normal distribution. The bit maps in Fig. 6 provide direct observations on such randomness with both location- and historical- independence.

D. Electrical Characteristics with Verification

Now that we understand the behavior of individual cells is unpredictable but the group behavior is well-predicted we have designed an operation algorithm as shown in Fig. 7. Instead of using conventional incremental step pulse programming (ISPP) we adopt a re-program approach with a fixed condition as shown in Fig. 8. The basic concept is that there is no need to increase the pulse height, since statistically a cell would be programmed to the desired range if we simply repeat the same program conditions. Such fixed condition can prevent overstressing the memory cells and also keep the array selectors/driver small.

For multi-level-cell (MLC) arrays the new algorithm can also reduce the chance of over programming compared to the traditional approach (Fig. 9). This is because in ISPP the median of the Gaussian distribution moves up due to higher applied pulses. By keeping the reprogram pulse at the same pulse height and only reprogram the failed bits the median stays unchanged (Fig. 7). Figure 10 clearly shows the effectiveness of the new algorithm applied to both RESET and SET operations, with trimming boundaries at 100 kΩ and 30 kΩ, respectively. The stable pass rates after each program-verify loop in Fig. 11 agree well with our earlier observation of the statistical nature after each programming pulse. The 1kb array resistance medians and standard deviations (Fig. 12), even for the first 10 run-in cycles, indicate the stability of the new operation algorithm.

E. Conclusions

Although it is hard to pinpoint individual bits after a programming pulse, the group behavior always follows Gaussian distribution and is predictable. An array operation algorithm is suggested based on this finding and is proven to effectively assure the memory window without overstressing the devices.

References

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- [3] Z. Wei, et al., *IRPS*, (2015) 5B-4.
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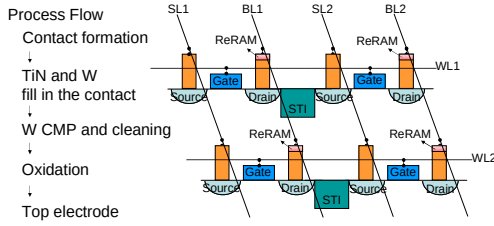


Fig. 1. Process flow of WO_x ReRAM and schematic layout of the 1T1R array structure.

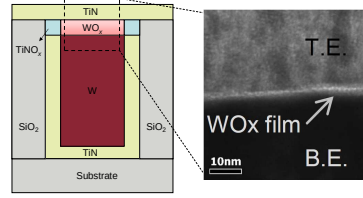


Fig. 2. Illustration of the TiN/ WO_x /W structure and the TEM image.

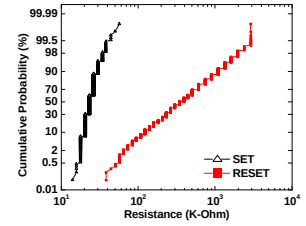


Fig. 3. Cumulative probability of the HRS and LRS for the 1 Kbit array.

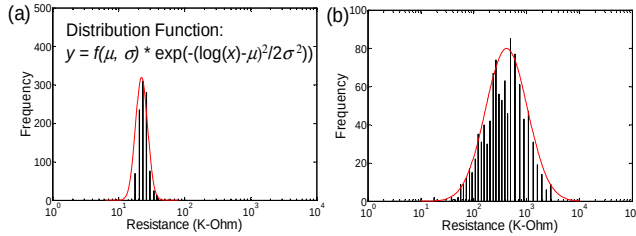


Fig. 4. (a) The LRS and (b) HRS distribution after one-shot SET and RESET pulse, fitted with Gaussian distribution curves.

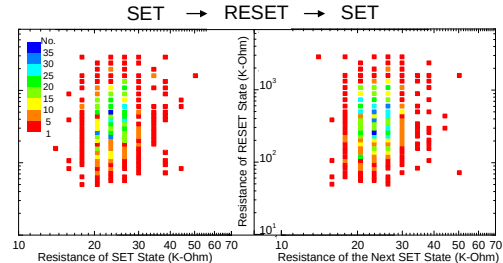


Fig. 5. The resistance tracking from SET → RESET → SET of the 1 Kbit array. It is hard to predict the resistance level of a cell after the next operation. Color bar: number of occurrences.

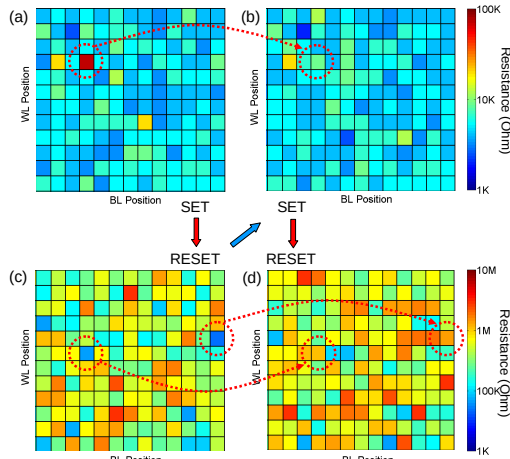


Fig. 6. The resistance bit-maps of two consecutive cycles. Note that for each cell the resistances levels are typically not the same after the next cycle.

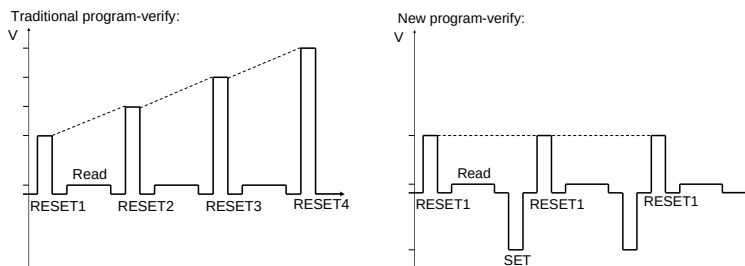


Fig. 8. Waveforms of the traditional (ISPP) and the new program-verify algorithm.

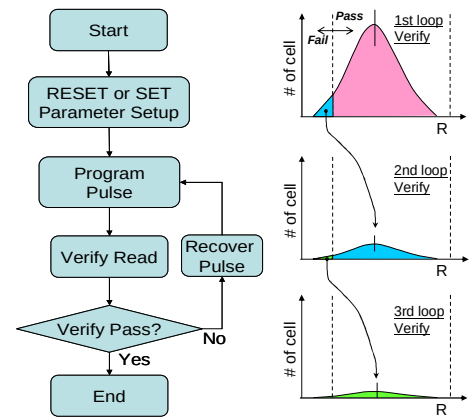


Fig. 7. The new program-verify flow with fixed program pulses. The shape and center of the resistance distribution remain the same after applying the re-program pulse to the verify-fail cells. The tail population is reduced after each re-program since only the failed bits are reprogrammed.

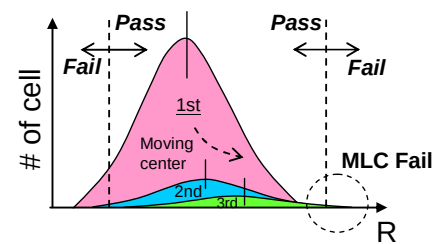


Fig. 9. Resistance distributions of re-programmed bits in the traditional flow. The moving distribution center increases the chance of failure in MLC array.

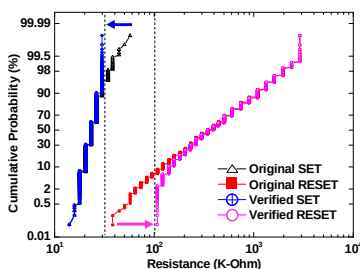


Fig. 10. Accumulated probability of the 1 Kbit array with the new operation scheme.

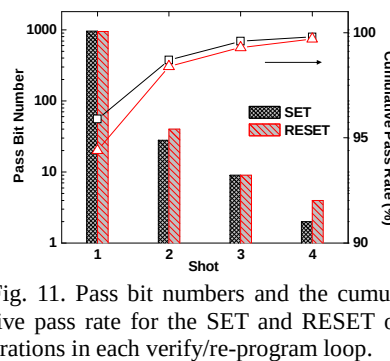


Fig. 11. Pass bit numbers and the cumulative pass rate for the SET and RESET operations in each verify/re-program loop.

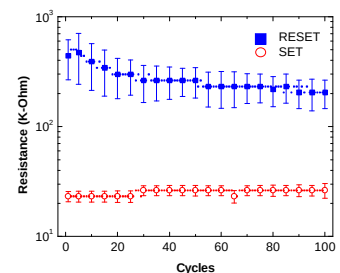


Fig. 12. Cycling history of the 1 Kbit array with the new operation algorithm.