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Spintronics memory devices for ultralow-power and high-performance integrated circuits

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Abstract

Spintronics memory devices, or MRAMs, offer a new paradigm of semiconductor technology. Here we review our recent studies on various spintronics devices being developed for nonvolatile very large-scale integrated circuits (VLSIs). Two-terminal device with spin-transfer torque switching and three-terminal devices with current-induced domain wall motion or spin-orbit torque induced switching are addressed. In particular, we discuss their properties exhibited at nanoscale dimensions.

1. Introduction

With the nonvolatility, fast-operation capability, virtually infinite endurance, and scalability, spintronics memory devices are regarded as not only a promising replacement for current semiconductor-based memories that have faced several serious issues, but also a key technology for next generation IoT (Internet of Things) society. Proof-of-concept demonstration has been recently shown by realizing nonvolatile microcontroller units with the use of spintronics devices [1, 2]. Spintronics devices have two structural variations: two-terminal device and three-terminal device (Fig. 1); the former is suitable for large-capacity memories whereas the latter is more suited for high-speed applications. For the magnetization switching scheme, a spin-transfer torque (STT) switching is utilized for the former, whereas a current-induced domain wall (DW) motion or spin-orbit torque (SOT) induced switching is utilized for the latter. In the following, we show our recent works on these two- and three-terminal devices, especially the properties at deep sub-100-nm dimensions where their unique physics can be revealed.

2. Two-terminal STT device

For two-terminal STT device, current passing through a magnetic tunnel junction (MTJ) gives rise to the STT and switch the magnetization of a recording layer (Fig. 1a). A CoFeB-MgO based MTJ with a perpendicular easy axis [3] has become a de facto standard material system since it satisfies a small critical current, reasonably large thermal stability factor, and large tunnel magnetoresistance ratio simultaneously [3]. A subsequently developed CoFeB-MgO MTJ with a double interface structure shows a thermal stability factor large enough to ensure the retention at the MTJ diameter of 20 nm [4,5]. The structure allows us to examine the switching at 11 nm. We find that in this scale the effective damping constant, to which the switching current is proportional, decreases with the MTJ size [6]. Very recently, we have also characterized the switching dynamics of single-domain scale devices using short current pulses down to 1 ns.

3. Three-terminal DW-motion device

In the DW-motion device, write operation is performed by applying current pulse that displaces a domain wall formed in a ferromagnetic recording layer (Fig. 1b) [7]. Since the high-speed capability is the prime advantage of the three-terminal cell circuits, which is obtained at the cost of cell size, the reliable DW motion at nanosecond timescale is of particular importance. The high-probability DW depinning from an artificially prepared potential well has been achieved by 2-ns current pulses using Co/Ni multilayer with a perpendicular easy axis, suggesting suitability for the VLSI applications [8]. Another unique feature of the DW-motion device recently revealed is the efficiency of current-induced motion with respect to the thermal stability factor. While its critical current scales along with the device size, thermal stability factor, which is independent of the critical current, increases as the device size decreases. As a result, the efficiency defined as the thermal stability factor divided by the critical current becomes larger as the device is miniaturized. We also find a critical length scale that demarcates the physics of thermally activated DW motion through the investigation on the dependence of thermal stability factor on the device size down to 20 nm [9].

4. Three-terminal SOT device

SOT induced switching is also applicable for the write operation of the three-terminal device (Fig. 1c). Recently, it

was found that an in-plane current applied to heterostructure with structural inversion asymmetry generates a torque, i.e., the SOT, which can switch the magnetization of ferromagnetic layer with both perpendicular and in-plane easy axes [10-13]. In spite of intensive studies, mechanism that determines the critical current density for switching has been highly controversial. We investigate the SOT switching using Ta/CoFeB/MgO structure with various sizes under various conditions. The device size we studied is down to 30 nm, where single-domain picture is expected to be applicable. This allows us to directly compare the experimental results with a macrospin theory and thus unambiguously discuss the factors that govern the switching. Through the systematic study, we find that the experimental results from the single-domain scale device are reasonably explained by considering both the Slonczewski-like torque and field-like torque [13].

5. Conclusion

We have clarified the physics governing the current-induced magnetization switching by reducing the device size down to 11 nm (STT device), 20 nm (DW-motion device), and 30 nm (SOT device). The gained insights allow us to properly design the spintronics devices and VLSIs, which promote the leading-edge CMOS technologies and also open a new era of ultralow power information technology.

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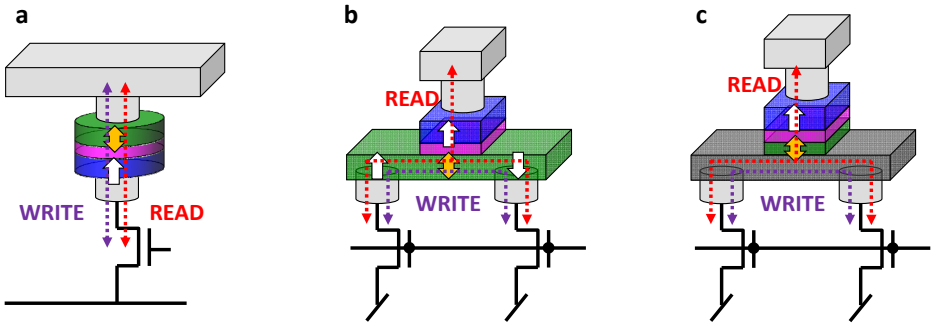

Fig. 1: Three kinds of spintronics memory devices addressed in this paper. **a**, Two-terminal spin-transfer torque (STT) switching device. **b**, Three-terminal domain wall (DW) motion device. **c**, Three-terminal spin-orbit torque (SOT) switching device.