180-mV Subthreshold Operation of Crystalline Oxide Semiconductor FPGA Realized by Overdriving Programmable Power Switch and Programmable Routing Switch

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Abstract

A crystalline oxide semiconductor (OS) FPGA capable of subthreshold operation is developed. To achieve subthreshold operation, the OS FPGA employs overdriving of a programmable routing switch and a programmable power switch for power gating by using OS FFT as an ideal floating gate with excellent charge retention. In a prototype chip fabricated with a 0.8-μm OS/0.18-μm CMOS hybrid process, while maintaining features realizing low power consumption proposed in our previous studies [1, 2], the following are shown: a configured combinational circuit operates at a minimum operating voltage (Vmin) of 180 mV, a configured sequential circuit operates at Vmin of 190 mV with 12.5 kHz, and the minimum power-delay product scores 3.40 pJ/operation at 330 mV.

1. Introduction

An FPGA is expected to be the optimal device for sensor networks if FPGAs can flexibly change their circuit configurations to operate at low voltage enough to use energy harvesting in the standby state and perform high-performance processing during signal processing after receiving a signal [3].

The oxide semiconductor (OS) FPGA [1, 2] is a multi-context FPGA having nonvolatile configuration memory (CM). It uses an ultra-low off leakage current of a crystalline OS FET, typically a c-axis aligned crystalline indium–gallium–zinc oxide (CAAC-IGZO) FET. The OS FPGA features fine-grained power gating (PG), normally-off driving, and fast context switching at low power consumption. Therefore, an OS FPGA driven at low voltage would be suitable for a sensor network application.

This paper proposes an OS FPGA appropriate for subthreshold operation realized by overdriving a programmable power switch (PPS) and a programmable routing switch (PRS) using a floating node that has an ideal charge retention function achieved by an OS FET. The method enables PPS overdriving without generating negative potential and provides a power-saving PRS with a high Ion/Ioff ratio.

2. Low-voltage Design of OS FPGA

In addition to a general design policy which limits the number of transistor stacks [4, 5] for subthreshold operation, an FPGA needs another design policy to overcome specific problems such as a threshold voltage drop of a pass transistor in a PRS and static leakage current due to a low Ion/Ioff ratio [3]. The OS FPGA [1, 2] is required to handle an additional issue, which is the substantial increase in the number of transistor stacks in a PRS for realizing PG for individual programmable logic elements (PLEs), which is the key technology for lowering power consumption.

To solve these problems, overdriving using a floating node that has a charge retention function formed with an OS FET is proposed. The concept of this construction is to boost the supply voltage only when configuration data are updated (Fig. 1).

In the PPS, data 1 or 0 (HVDD or GND) are written to Ncfg for configuration and to Nctx for context switching. Then, by turning off the OS FETs (MOcfg and MOctx), Ncfg and Nctx become floating and retain the potential. At this time, the HVDD domain can be power gated. Thus, the pass transistors keep a high Ion/Ioff ratio and retain high potential at ultra-low power [1, 6].

In the PPS, the OS FET (MOcfg) is turned off, causing Ncfg to float. Here, when the voltage of the LVDD domain is changed from a high potential (LVDDh) to a low potential (LVDDD), the potential of Ncfg is lowered via capacitive coupling between the PPS gate and the LVDD wiring through a parasitic capacitor. That is, overdriving is possible without a power source circuit generating negative voltage.

In low-voltage driving, application of a slight negative potential to the PPS gate greatly improves performance, indicating effectiveness in low-voltage operation (Fig. 2).

Fig. 3 shows a block diagram of the FPGA; a timing chart for the CM; and circuit diagrams of a PLE, PRS, PRSs, CM. Power is supplied to the entire HVDD domain in configuration mode, and supplied only to the context controller in context switch mode. The circuits in the HVDD domain are not used in normal mode; thus, power supply is stopped by PG.

3. Measurement Results

The OS FPGA and a PLE test element group (TEG) are fabricated with a 0.8-μm OS/0.18-μm CMOS hybrid process. Fig. 4 shows Ig–Vg curves of the OS FETs.

First, the operation of the PLE TEG at LVDD of 180 mV, which is the minimum operating voltage (Vmin), is confirmed in configuration of a 4-input AND or 4-input OR (Fig. 5). LVDDh is 2.5 V when configuration data are updated.

Then, the operation of the OS FPGA chip is confirmed. Figs. 6 and 7 show the LVDD dependence of the maximum operating frequency (Fmax), power consumption, and a power-delay product (PDP) of the OS FPGA in a three-stage ring oscillator (RO3) and a 4-bit counter (CNT4) configuration, respectively. Here, non-active PLEs are power gated by fine-grained PG. LVDDh is 1.2 V and HVDD is 2.5 V. Vmin and the minimum PDP (PDPmin) of the OS FPGA are 180 mV with RO3 configuration and 3.40 pJ with CNT4 configuration at LVDD of 330 mV and Fmax of 28.6 kHz. PDPmin is approximately 49% lower than that of an SRAM FPGA [7] (Table I). The results also show that Fmax increases from 33.3 kHz to 8.6 MHz at 900 mV, that is Vmin of the previous OS FPGA [1, 2]. Therefore, the present OS FPGA achieves low-power driving and high-performance processing.

To determine the contribution of the overdriving, the difference in PDP with and without overdriving is evaluated using the CNT4 configuration (Fig. 8). The overdriving lowers Vmin from 390 mV to 180mV and decreases PDPmin by 24% from 4.48 pJ at 390 mV to 3.40 pJ at 330 mV.

A context switch from CNT3 to CNT4 configuration in single clock is performed on the condition where the PDP of the CNT4 configuration is the lowest (330 mV, 28.6 kHz) (Fig. 9). Here, the output signals boosted from LVDD to 2.5 V by level shifter are monitored. The energy required for the context switching of the OS FPGA is estimated at 6.42 nJ, and average power of CNT3 is estimated at 3.86 μW by SPICE. If contexts switch once every second, the power is less than 0.17% of that in operation; thus, the energy overhead is extremely small, even when the supply voltage is boosted in configuration data update.

To assess the duration of the overdriving effect, a temporal...
change of oscillator frequency in RO3 configuration is evaluated (Fig. 10). Without context switching, the frequency decreases by only 4.5% in four hours. Furthermore, one refresh operation per hour reduces an oscillation frequency variation to 1.0% or less and enables the overdriving to be maintained.

4. Conclusions

The OS FPGA driven at a subthreshold voltage of 180 mV is realized by overdriving the PPS and PRS using a floating node with ideal charge retention characteristics that is realized by an OS FET with an ultra-low off-state current. The OS FPGA is still having the features of the previous one, such as low power consumption in standby mode due to fine-grained PG and nonvolatile CM and fast context switching. The OS FPGA promises to be highly suitable for a sensor network device.

References