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# Interface Engineered $HfO_2$-based 3D Vertical Resistive Random Access Memory with Forming-Free Operation

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**Abstract**

**We demonstrate a 3D vertical resistive random access memory (RRAM) by implementing a Pt/$HfO_2$/TiN memory cell with $HfO_2$ grown by atomic layer deposition (ALD). In-situ interface engineering results in forming-free operation and allows non-linearity tuning by current compliance (CC). The vertical RRAM shows excellent read and write disturb immunity between vertically stacked cells, retention over $10^4$ s and excellent switching stability at 125 °C, as well as 10 ns switching speed.**

## 1. Introduction

Because of its simple structure and CMOS technology compatibility, oxide-based RRAM is an attractive candidate for future storage class memory [1]. A vertical RRAM structure is currently the only technological pathway which enables ultrahigh bit density beyond the established 3D NAND Flash [2]. Besides reliability concerns related to its stochastic nature, two major bottlenecks for oxide-based RRAM implementation are the necessity of forming procedure and the requirement of an additional selection device for suppressing the sneak currents in crossbar arrays (Fig. 1). The latter can be solved by engineering sufficient non-linearity of the cell resistance, as recently shown on the TiN/$HfO_2$/Pt device [3]. In this work we present a vertical RRAM device with an in-situ engineered $HfO_2$/TiN interface by $O_3$ treatment. The device exhibits significantly reduced forming voltage enabling the forming-free operation in the AC pulsed mode and the non-linearity tuning by CC during SET. We demonstrate sufficient retention, read and write disturb immunity between vertically stacked cells and 10 ns switching speed.

## 2. Experimental

The fabrication process flow of the 3D vertical RRAM structures is described in detail in Fig. 2, with a TEM image of the finished structure in Fig. 3. Because of the CMOS-compatible TiN dry etching, a much steeper vertical profile of $SiO_2$/TiN/$SiO_2$/TiN/$SiO_2$ pillars was achieved as compared with the previous TiN/$HfO_2$/Pt device [4] using Pt as the horizontal electrodes. 5-nm thick $HfO_2$ switching layer was deposited at the vertical sidewall by ALD using the TEMAHf precursor and ozone at 300 °C [3]. Pre-treatment of the TiN electrodes by ozone was performed in-situ. The Pt vertical electrodes of various line widths (2 – 100 μm) were evaporated using electron gun and patterned through a lift-off process. The area of a smallest sidewall device was 0.2 $\mu m^2$.

## 2. Results and discussion

The ozone pre-treatment of the TiN electrode forms an interfacial $TiO_xN_y$ layer with a critical oxygen vacancy profile (Fig. 4). The inset in Fig. 5 shows the reduction of the forming voltage below -2 V by ozone pretreatment. Moreover, as shown in Fig. 5, the non-linearity of the low resistance state (LRS) can be tuned to up to ~10 (at 0.8 V read) if sufficiently low (300 μA) CC is applied. Non-linear LRS is probably related to the $TiO_xN_y$ interfacial layer [4]. The switching currents were independent of the cell area, suggesting a filamentary switching mechanism. Stable switching parameters of the both top and bottom cells in self-compliant (no CC applied) regime are shown in Figs. 6 and 7. Cells stably operated even at 125 °C (Fig. 7), with satisfactory retention (Fig. 8). Fig. 9 shows robust read and write disturb immunities between the adjacent top and bottom cells during concurrent switching of both cells.

Devices fabricated using ozone pre-treatment were able to operate under the AC pulsed mode without prior forming or DC training (Fig. 10). To achieve stable operation down to the 10 ns speed, the amplitude of the reset pulse had to be increased accordingly (Fig. 11). Devices show high endurance with memory window of ~10× after $10^6$ (Fig. 12), and window of ~3× after $10^7$ pulses of 100 ns pulse width.

## 3. Conclusions

We demonstrate a 3D vertical Pt/$HfO_2$/TiN RRAM. The $HfO_2$/TiN interface engineering allowed the forming-free operation in the pulsed mode and non-linearity tuning by CC.

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**References**

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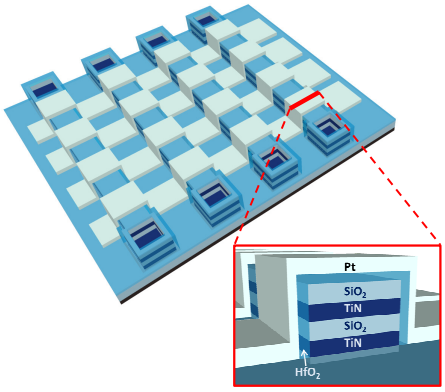


Fig. 1: Two-layer 3D vertical RRAM array. Pt/$HfO_2$/TiN memory cells are defined on the sidewall of the stacked TiN electrodes.

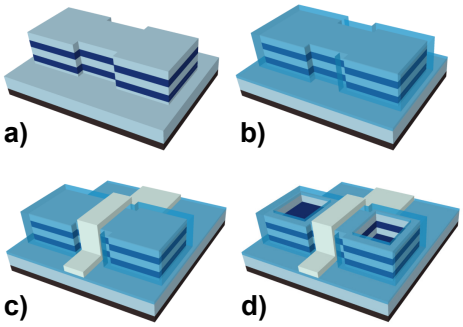


Fig. 2: Fabrication flow: a) $SiO_2$/TiN multilayer etching, b) $HfO_2$ ALD, c) Pt top electrode deposition and lift-off, and d) contact holes etching.

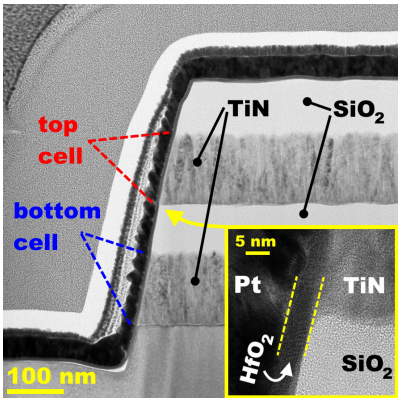


Fig. 3: TEM image of the two-layer 3D vertical stack steep side-wall profile. Inset shows the 5-nm thick $HfO_2$ detail.

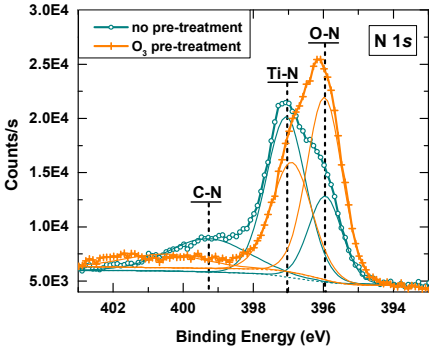


Fig. 4: Surface XPS spectra of the N 1*s* peak show an increased O-N peak intensity at the expense of the Ti-N peak after pre-treatment with $O_3$, suggesting a $TiO_xN_y$ layer formation on the TiN surface.

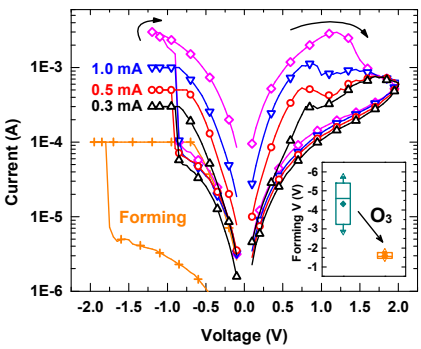


Fig. 5: DC IV sweeps of the Pt/$HfO_2$/TiN memory cell. LRS current and non-linearity can be controlled by CC. Inset: Reduction of the forming voltage to only -1.5 V using the $O_3$ pre-treatment.

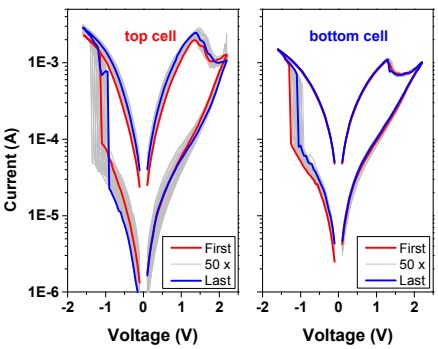


Fig. 6: Stable bipolar resistive switching of the adjacent top and bottom cells in the self-compliant regime (without using CC). Both cells show excellent stability of the DC IV loops.

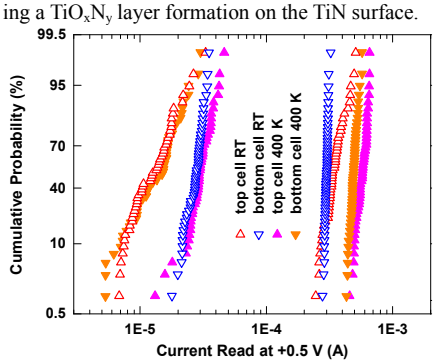


Fig. 7: Cumulative probability distribution of the low and high resistance state currents for adjacent top and bottom cells, both showing satisfactory resistance ratios also at 125 °C.

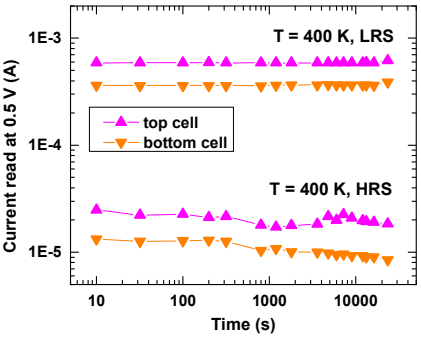


Fig. 8: Retention of the adjacent top and bottom cells, operated and monitored simultaneously at 125 °C for ~7 hours. No degradation of the memory states was observed.

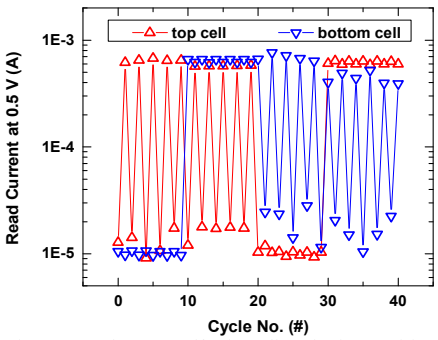


Fig. 9: Robust read/write disturb immunities shown for the adjacent cells during concurrent switching. All four scenarios were measured, each for 10 cycles.

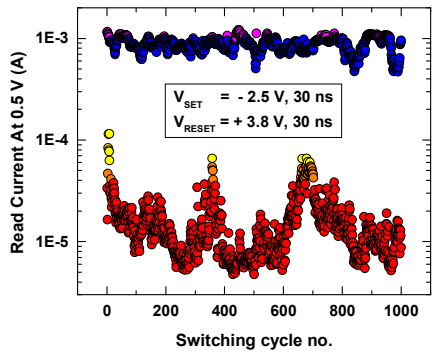


Fig. 10: AC pulsed mode operation using pulses of 30 ns width with 10 ns rise and fall times, without prior forming nor DC training. Device was read after each pulse using 100 µs read pulse of 0.5 V.

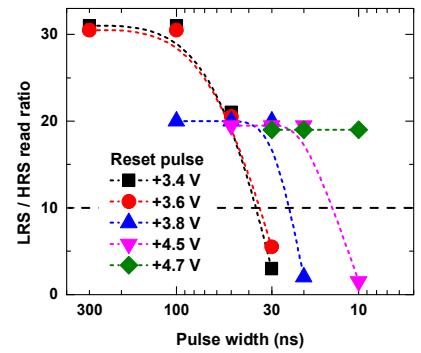


Fig. 11: Trade-off between reset pulse amplitude and pulse width. To obtain switching in the ultra-fast range down to 10 ns, higher reset pulses are necessary. SET pulse of -2.8 V was enough.

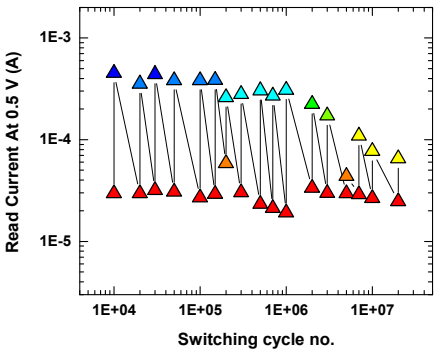


Fig. 12: Devices show high endurance with memory window of ~10× retained after $10^6$ pulses, while still showing a window of ~3× after $10^7$ pulses. 100 ns wide pulses were used.