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Investigation of Carbon Nanotube Memory Cell Array Program Characteristics

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Abstract

A 4 M-bit carbon nanotube (CNT) based non-volatile memory (NRAM) cell array is measured to investigate program characteristics. In detail, first, reset is measured by controlling the program voltage and current independently. Reset is found mainly dependent on the program voltage rather than the program current. Next, 10^8 write cycles are applied to the memory cell array and no cell array wear-out or broken cell is found. Finally, program characteristics of two verify-reset schemes are compared. The maximum verify-reset voltage can be reduced by increasing the number of reset pulses.

1. Introduction

The resistance switching in NRAM is attributed to the modulation of distance and tunneling current between CNTs [1]. The NRAM single cell has demonstrated > 10^{11} program endurance, 20 μA program current and potential of multi-level cell [2], which make NRAM a strong candidate for next generation non-volatile memories. In [3], a 4 M-bit 250 nm NRAM cell array is measured to show basic NRAM cell array program characteristics, such as 50 ns access time, cell read current over 10^4 write cycles, 15 μA cell program current and resistance distributions before and after 120°C, 24 hours data retention. However, the characteristics of program error and verify-program scheme are not investigated. In this work, a 4 M-bit 116 nm NRAM cell array is measured. The program characteristics, such as program error and verify-reset scheme, are investigated for the first time. In specific, first, reset bit error rate (BER) is measured by controlling reset voltage and current independently. Reset is found more dependent on the program voltage rather than the program current. Furthermore, no wear-out or broken cell is found after 10^8 write cycles. Lastly, the program characteristics of two verify-reset schemes are compared. The maximum verify-reset voltage can be reduced by increasing the number of reset pulses.

2. NRAM Single Cell Program Characteristics

The mechanism of NRAM cell resistance switching is shown in Fig. 1 [1]. The distance between CNTs can be decreased and increased during set and reset, respectively, which changes NRAM cell tunneling current and resistance during read [1]. In Table 1, the measurement on single NRAM cell [2] shows higher program endurance and lower program current compared with Al_xO_y based Resistive Random Access Memory (ReRAM) [4] and Phase-change RAM (PRAM) [5], [6].

3. NRAM Cell Array Program Characteristics

Fig. 2 shows the photograph of 4 M-bit NRAM test chip [3]. The memory cell array structure is shown in Fig. 3 [3]. Fig. 4(a) shows that reset voltage and current can be changed independently by controlling the source-line (SL) and word-line (WL) voltages. In Fig. 4(b), reset BER decreases by increasing the program voltage (SL voltage), even when the current is low (WL voltage is low). As a result, reset is more dependent on the program voltage compared with the program current. Fig. 5 shows a verify-set [2] scheme and two verify-reset [2] schemes which are measured in this paper for the cell array program. The verify-set and verify-reset scheme 1 increase program voltage monotonically. On the other hand, the single NRAM cell can effectively reset by applying multiple reset pulses with fixed voltage [2]. Similarly, in the verify-reset scheme 2 the maximum reset voltage is fixed at the predetermined value and the number of pulses with fixed reset voltage increases to reduce BER. From Fig. 6 to Fig. 8, the verify-reset scheme 1 is used. Figs. 6(a) and 6(b) compare measured BER reduction during verify-set and verify-reset, respectively, after 10^3 and 10^8 write cycles [3]. The NRAM cell array does not wear-out after endurance [3]. Fig. 7 shows the measured NRAM cell array set and reset BERs after verify-program. Each data point is the maximum BER in 5 continuous write cycles. Between two data points, set and reset pulses are repeated without using verify-program scheme to save the measurement time. The reset BER is dominant over 10^8 write cycles compared with set BER. Figs. 8(a) and 8(b) show measured set and reset error rates of each NRAM bit after 10^8 write cycles. No broken cell is observed.

In Fig. 9, two NRAM cell array verify-reset schemes are measured. Compared with the verify-reset scheme 1, the maximum program voltage is lower in the scheme 2 and similar reset BER is obtained by applying more program pulses. Fig. 10 compares the cell array program scheme by using different memory cell array structures [7]. The common source-line (SL) architecture achieves the high density array. Reset pulses are applied to cells connected to the common source-line. In this work, the common source-line architecture is assumed to evaluate the NRAM cell array program time. Table 2 summarizes the NRAM cell array program characteristics. First, the reset program is mainly dependent on the SL voltage. Second, reset error rate is higher than set error rate. No broken cell is found after the 10^8 write cycles. Third, tradeoff of maximum reset voltage and program time is observed in two verify-reset schemes. The scheme 1 has shorter program time but higher reset voltage. In contrast, the scheme 2 has lower reset voltage but longer program time.

4. Conclusion

This paper shows the first comprehensive analysis of the program characteristics of 116 nm, 4 M-bit NRAM cell array. Two verify-reset schemes are compared to show the tradeoff between the maximum reset voltage and the program time.

Reference

[1] T. Rueckes, *Int. Tech. Roadmap for Semiconductors*, 2013, presentation. [2] S. Ning et al., *Symp. on VLSI Tech.*, 2014, pp. 120–121. [3] G. Rosendale et al., *European Solid-State Circuits Conference*, 2010, pp. 478–481. [4] S. Ning et al., *Solid-State Electronics*, vol. 103, pp. 64–72, Jan., 2015. [5] H. Y. Cheng et al., *IEEE Int. Electron Devices Meeting*, 2013, pp. 30.6.1–30.6.4. [6] K. Johguchi et al., *IEEE Int. Reliability Physics Symp.*, 2013, pp. MY.5.1–MY.5.4. [7] B. Zhao et al., *Design, Automation and Test in Europe*, 2012, pp. 1451–1454.

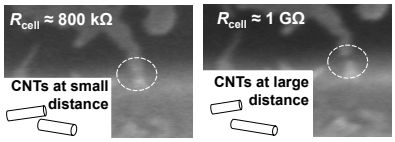


Fig. 1 SEM photographs of carbon nanotube (CNT) based memory (NRAM) cell with different resistances [1]. Cell resistance is small when CNTs has small distance (left). In contrast, cell resistance is large when CNTs has large distance (right).

Table 1 Comparison of NRAM, Al_xO_y ReRAM and PRAM single cells. NRAM cell has higher endurance and smaller program current.

	NRAM [2]	ReRAM [4]	PRAM [5]
Material	Carbon nanotube (CNT)	Al_xO_y	$Ge_2Sb_2Te_5$
Resistance switching mechanism	Tunneling current between CNTs	Filament size	Material phase
Endurance	> 10^{11}	10^7	10^9
Program current	20 μA	100 μA	150 μA

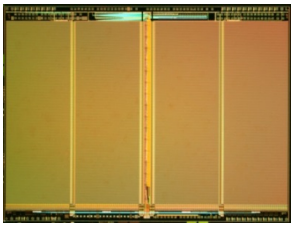


Fig. 2 Photograph of NRAM test chip [3].

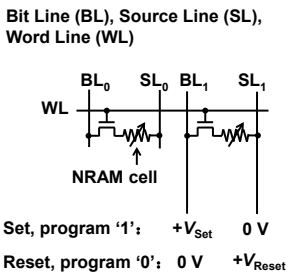


Fig. 3 NRAM cell array structure and programs [3].

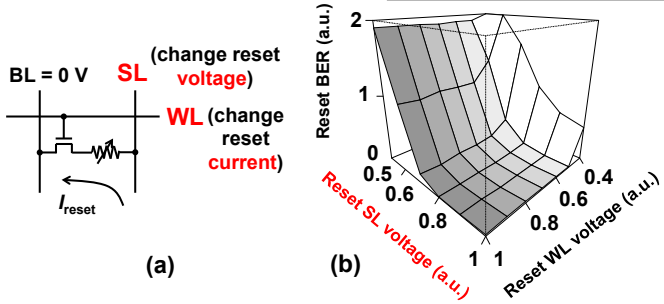


Fig. 4 (a) One pulse reset by changing program voltage and current independently. (b) Measured 256 Bytes NRAM cell array reset bit error rate (BER). Reset errors is mainly dependent on source-line (SL) voltage.

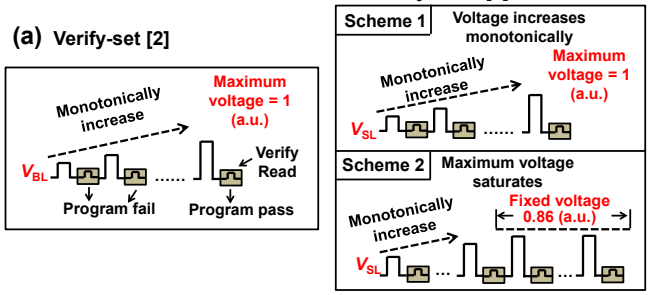


Fig. 5 (a) Verify-set scheme and (b) two verify-reset schemes. The Program voltage increases monotonically in verify-set and verify-reset scheme 1. In contrast, verify-reset scheme 2 has lower maximum voltage and more reset pulses than the scheme 1.

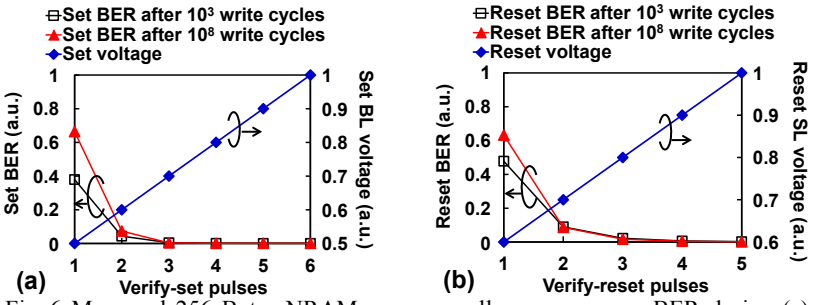


Fig. 6 Measured 256 Bytes NRAM memory cell array program BER during (a) verify-set and (b) verify-reset. NRAM cell array does not wear-out after 10^8 write cycles. The verify-reset scheme 1 in Fig. 5(b) is used.

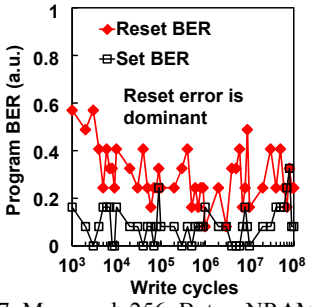


Fig. 7 Measured 256 Bytes NRAM cell array program BER over 10^8 write cycles. Reset error is more than set error. The verify-reset scheme 1 is used.

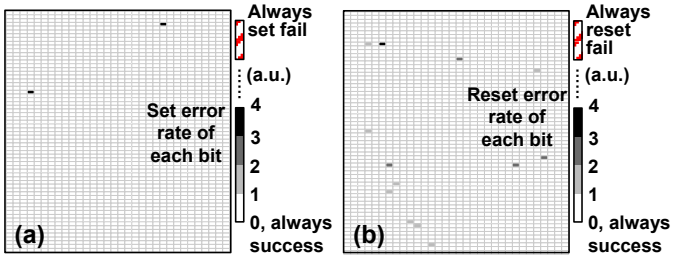
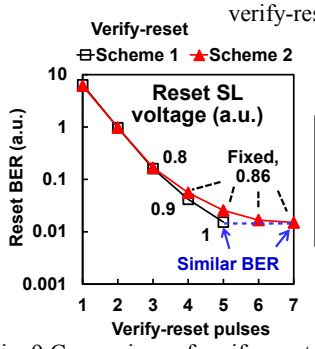


Fig. 8 Measured (a) set and (b) reset program error rates of each NRAM bit (total 256 Bytes) after 10^8 write cycles. No broken cell is observed. The verify-reset scheme 1 is used in this measurement.



Verify-reset [2]	Reset SL voltage (a.u.)	Pulses	Reset BER (a.u.)
Scheme 1	1	5	1
Scheme 2	0.86 (lower)	7	0.98

Similar BER

Fig. 9 Comparison of verify-reset characteristics. The scheme 1 has higher maximum voltage and uses less reset pulses. In contrast, the scheme 2 has lower voltage and uses more reset pulses.

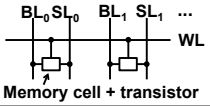
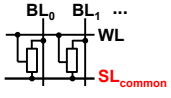
Divided source-line architecture [7] (low density array, fast program)	Common source-line architecture [7] (high density array, slow program)
Low density 	High density 
One-step program, fast — User data ⇨ Set and reset simultaneously	Two-step program, slow — User data ⇨ Set ⇨ Reset

Fig. 10 Comparison of cell array program time. The common source-line architecture is assumed to evaluate the NRAM cell array program time. In this architecture, verify-set and verify-reset are applied in serial [7].

Table 2 Summary of NRAM cell array program characteristics.

1. Reset program (Fig. 4)	Mainly depends on SL voltage			
2. Error analysis (Fig. 8)	Reset error is dominant. No broken cell after 10^8 write cycles			
3. Verify-reset schemes [2] (Fig. 9)		Maximum reset SL voltage (a.u.)	✱ Set + reset time (a.u.)	Set + reset BER (a.u.)
	Scheme 1	1 (high)	1 (short)	1
	Scheme 2	0.86 (low)	1.18 (long)	0.99 (similar)

✱ Assume using the high density array, as shown in Fig. 10.