Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp1224-1225

Generation of highly stable microwave from a spin torque oscillator by phase locked loop

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Abstract

We built a phase locked loop (PLL) circuit using a spin torque oscillator (STO) as a voltage controlled oscillator (VCO), which generates a 5.12 GHz microwave signal phase locked to an 80 MHz reference signal. When the STO is under free running oscillation, its spectrum showed a line width of about 6.4 MHz, corresponding to a quality factor of about 800. Once it is phase locked, the line width becomes extremely narrow, less than the measurement limit of 1 Hz. This is a clear signature of successful phase locking of the microwave signal generated by the STO to the reference signal.

1. Introduction

Various modern electronics systems require multiple radio frequency (RF) signal sources, often in microwave frequency range, with very low phase noise. Spin torque oscillators (STOs) are a promising candidate for such RF signal sources that can be directly integrated into semiconductor chips with an extremely small footprint, which should lead to significant benefit in terms of packing density and fabrication cost. However, performances of STOs, such as the output power and quality factor (Q factor) under free running oscillation, have not been good enough for most practical applications yet.

Regarding phase noise, a technique called injection locking has successfully stabilized oscillation frequency (f_{STO}), in which a microwave power from a reference source with identical or integer multiple of the oscillation frequency ($f_{Ref} = n\, f_{STO}$, where n is an integer) is directly injected into the STO. As a result, an extremely narrow line width, i.e. low phase noise, was achieved [1]-[4]. Unfortunately, this technique is not a commercially viable option because of the necessity to have another RF reference source.

In contrast, phase locked loop (PLL) is widely used in real electronics systems to stabilize the frequency. In PLL, an RF signal is phase locked to a low frequency reference clock with low phase noise generated by a crystal oscillator, which is typically in 10-100 MHz frequency range ($f_{STO} >> f_{Ref}$). However, it has been difficult to implement an STO into a PLL circuit because of the large phase noise of STOs, especially when f_{Ref} is much lower than f_{STO} [5][6].

In this work, we have developed a PLL circuit implementing a high performance STO into it, and confirmed successful phase locked oscillation. Phase locked loops are used in many modern electronics systems, and the successful implementation of a STO based PLL demonstrated in this work should be a major leap toward practical microwave application of STOs.

2. Description about STO based PLL

The STO consists of a magnetic tunnel junction (MTJ) having an in-plane magnetized reference layer and perpendicularly magnetized free layer [7][8]. This STO shows a very high power and Q factor simultaneously, thanks to a large magnetoresistance (MR) ratio of the MTJ stack and absence of edge effects in the perpendicular free layer magnetization, respectively. Fig. 1 shows a block diagram of the PLL built in this work. A STO showing a Q factor of about 800 under free running oscillation and red shift for a small change of bias voltage is nominally biased through a pick-off tee to generate a 5.12 GHz microwave signal. This signal is amplified by a broadband low noise amplifier (LNA), and its frequency is down converted to 80 MHz by a 1/64 down counter. This signal and 80 MHz reference clock are fed to a phase frequency detector (PFD), which outputs a voltage signal proportional to the phase difference between the two signals (phase error signal, PES). The PES is low pass filtered and fed back to the bias control circuit to fine tune the STO frequency. That way, the phase of the STO output should be locked to that of the 80 MHz reference clock.

Fig. 2 shows the power spectrum of the STO output stabilized by the PLL mechanism. An extremely narrow oscillation peak, whose width is actually below the measurement limit of the spectrum analyzer (<1 Hz), is observed right at 5.12 GHz. This indicates that the PLL successfully locks the phase of the STO output to the 80 MHz reference clock, and the Q factor of the STO output is increased from

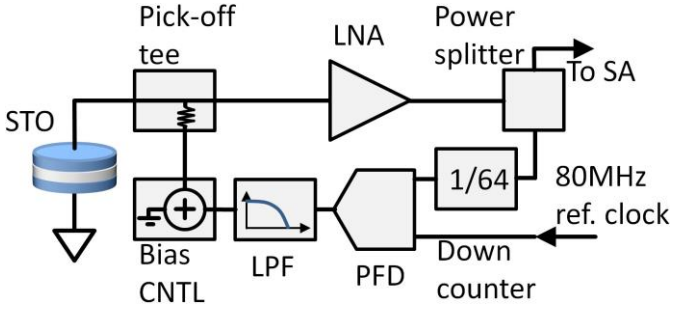

Fig. 1 Block diagram of the phase locked loop built in this work.

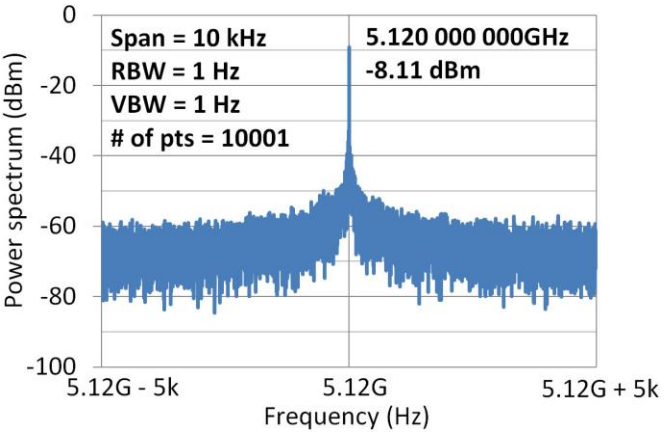

Fig. 2, Spectrum of the STO output signal stabilized by PLL.

800 up to as large as more than $5x10^9$ once the PLL is locked, reflecting the high stability of the reference clock source. This is the first demonstration of phase synchronization of a STO output to a lower frequency external signal. We also took a close look at the waveform of the STO output signal, and found that the phase locking in this PLL is still intermittent. This is considered to be because the frequency fluctuation of the STO in free running oscillation is so large that mode locking is occasionally lost. In the presentation, we will discuss the challenges in designing and building a PLL circuit using a STO, and the requirements on the STO performance for achieving a stable phase locked operation, based on the experimentally measured PLL characteristics. The successful locking of the STO output to a reference clock of much lower frequency by PLL mechanism demonstrated in this work should be a major milestone toward real practical applications of STOs to various electronics systems, and the results obtained in this work are expected to serve as guidance for the future development of STOs.

References

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