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Low Power Electronics beyond 5nm

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Abstract

Power dissipation has become the major challenge for the current CMOS technology. This is due to the voltage scaling which is limited by the subthreshold slope on the one hand, and on the other the volatile CMOS demands for power-on to maintain the state. This talk will address the potential directions as well as the current progress for future low-power electronics beyond 5nm. Among them are tunnel field-effect transistors based on novel 2D materials, and non-volatile spintronics and their integration with CMOS to resolve the two major limits. Finally, nano-architectures for different nanodevices will be discussed.

1. Challenges of continuing scaling

Over a billion times of improvements of CMOS technology in the past half century have changed our daily life, particular in data and information processing. Can we or for how long can we sustain this unprecedented progress in the history of mankind? One major challenge, namely power dissipation has surfaced. Due to the operation principle of conventional metal-oxide-semiconductor FET (MOSFET) that requires the thermionic injection of electrons over an energy barrier, the turn-on voltage (V_{th}) cannot scale-down well due to the theoretical nonscalable *kTln10* or 60 mV/dec sub-threshold swing (SS) limit at room temperature as illustrated in Fig. 1(a), thus leading to non-scalable dynamic power consumption[1]. Meanwhile, as the device size approaches the sub-5nm regime where quantum effects dictate device performance, the tunneling current between the source (S) and the drain (D), and the leakage currents from the gate-oxide layer and in the sub-threshold regime will contribute to a larger static power consumption, as summarized in Fig. 1(b)[2]. Thus, the search for low-dissipation solutions at the device, circuit and system levels is critical to the future advance of data and information processing and electronics industry.

2. Approaches

2D Tunnel Field-Effect Transistor

For CMOS logic electronics, the key figures of merit are both low OFF current (minimize leakage current) and low threshold voltage (but keep a sufficient ON/OFF ratio). In this regard, it has been argued that tunnel field-effect transistors (TFETs) might be one of the most promising candidate, among others. However, the major drawback of current TFETs development is their low ON-current limited by the band-to-band tunneling probability[3]. To address this issue, one has to reduce the tunneling barrier thickness so as to give a higher electric-field over the tunneling regime.

In additional to known approaches, I will discuss the use of the emergent 2D transition metal di-chalcogenides (TMDs) materials in the TFETs as illustrated in Fig. 2(a). Such TMDs are atomically thin semiconductors with weak van der Waals bonding between neighboring layers. Recently, it was calculated that with a monolayer TMD (i.e., WTe_2) TFET, high ON-current and low OFF-current could be expected, as illustrated in Fig. 2(b) [4]-[5]. Most importantly, given the ultra-thin channel thickness and a relatively small dielectric constant, the short-channel effect (with typical scaling length ~ 2nm) can be minimized; it thus offers promise for such TMDs-based TFET in the sub-5nm regime. Nevertheless, such predicted salient features of 2D TFETs have yet to be verified. The challenges include the still many material growth control issues; for example, can FINFET structures be realized with vertical growth of TMD FINs? Efforts may also be focused on the device design including the choice of bandgap, control of doping and realizing the S/D contact,).

Non-Volatile Spintronics

Spintronic devices, i.e., those utilizing the interactions of charge and spin, may offer a solution to alleviate the static power dissipation[6]. In particular, due to their inherent nonvolatility, these devices may allow for powering off when not in use without loss of information, hence potentially eliminating the standby power issue. Accordingly, spintronics has been proposed both as a complement to CMOS for hybrid CMOS-magnetic logic, as well as a means to realize various fully magnetic devices for beyond CMOS computing.

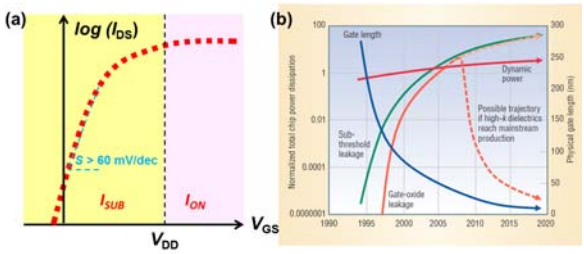

Fig. 1 Limited performances of Si-based MOSFETs. (a) Sub-threshold behavior, where the current follows an exponential relation with respect to the gate voltage with a slope always larger than 60 mV/dec. (b) Total chip dynamic and static power dissipation trends.

In the area of dilute magnetic semiconductors, the control of the magnetic properties by an electric field has been demonstrated at room temperature when quantum confinement in nanostructures is invoked [7]. By utilizing such an effect, a proposed nonvolatile transfer spin transistor (transpinor) may allow the manipulation of the spin state of the channel through a voltage rather than current flow and transfer the magnetic moment of the source to the drain, as shown in Fig. 2(c), different from earlier proposed devices. This transpinor could provide several important advantages over CMOS devices, including a low V_{th} and nonvolatility (stored as the magnetization of nanomagnets), to achieve lower power dissipation along with more functionalities (through spin freedom, gate-controlled ferromagnetism, and the critical behavior in a ferromagnetic phase transition)[8]. However, it is difficult to adapt it since it requires a change of the front end technology. The recent advent of a spin-transfer

torque magnetic random access memory (STT-MRAM)[9] with different variations has become commercialized. For this metallic non-volatile magnetic memory, the advantage is easy integration with CMOS in the backend of processing.

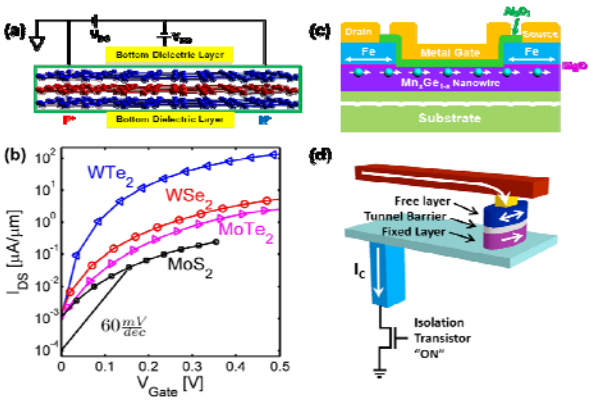

Fig. 2 Two-D material tunnel field-effect transistor and non-volatile spintronic devices. (a) Schematic of 2D TFET using TMDs as the channel materials. (b) Theoretical transfer characteristics of TMD TFETs with a high ON/OFF ratio and a steep SS below 60 mV/dec. (c) Schematic of non-volatile transpinor based on voltage-controlled magnetism. (d) Schematic of STT-MRAM.

Magnetoelectric and spin-orbit-torque

To further improve the energy efficiency and the density beyond STT-MRAM, additional concepts will be discussed: the use of voltage control of the magnetic anisotropy, or VCMA and strain mediated voltage control. Since the switching is enabled through voltage instead of large driven current, and the new magnetoelectric memory (MeRAM) can be readily integrated with CMOS

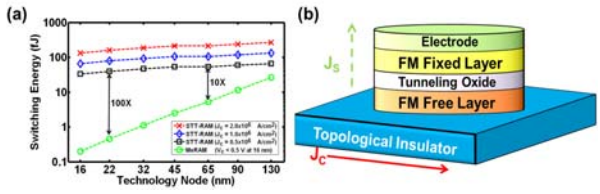

Fig. 3 Beyond STT-MRAM. (a) Comparison of switching energy (per bit) scaling for both the MeRAM cell and STT-MRAM cell. (b) Three-terminal device configuration exploiting the giant SOT in TI heterostructures. The Switching current and read out MTJ current are separated and the write energy can be much reduced.

similar to STT, but can simultaneously achieve high density as well as ensure the scalability to smaller dimensions, as displayed in Fig. 3(a) [10].

Next, I will describe the recent discovery of a giant spin-orbit-torque (SOT) realized in novel semiconductors like topological insulators (TIs) [11]. Due to the large spin-orbit interaction and unique spin-momentum-locking feature, the spin current along the TI surface can apply efficient SOT to the adjacent magnetic layer, thus leading to magnetization switching with a critical switching current orders of magnitude smaller than STT-MRAM. Therefore, with MeRAM and SOT, novel spintronic memory and logic may be ultimately constructed to have energy budgets of much less than 1 fJ/operation.

Integration of COMS with all metal spintronics

Finally, the outlook of nonvolatile circuits with hybrid CMOS and spintronics for new circuits and architectures will be discussed. With magnetic inherent nonvolatility and re-configurability along with high endurance, high density, low energy, the replacement of low density SRAM may afford a migration from the today's logic dense scenario to memory intensive CPU. New computation paradigms may emerge. It is also possible to invoke magnetic non-volatile logic (NVL) with CMOS or simply with all magnetics for energy-efficient and for realizing instant-on nonvolatile systems. For the latter, a possible avenue of using spin wave logics will be discussed [12].

3. Conclusions

In this talk, possible low power electronics beyond 5nm were discussed. Combining the strength from both the tunneling and the van der Waals structure, the TMD TFETs show great promise in terms of high on current density, ON/OFF ratio and sharp SS. Meanwhile, the unique non-volatile, electric-field-controlled magnetic properties will enable us to design novel spintronic devices for high density and energy efficiency. The integration of spintronics, particularly nanomagnetics with CMOS may offer the first solution to reduce the standby power dissipation. The use of 2-D materials may also promote potential 3-D monolithically integration if the backend processing compatibility can be fully established. This may afford layers of high performance active CMOS based on 2-D materials to be built on top of Si CMOS. Nanoarchitectures involving the use of high density of magnetic memories and logic circuits may lead to energy efficient new design of computational and information processing systems.

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