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# Introduction of SiGe/Si Heterojunction into Novel Multilayer Tunnel FinFETs

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**Abstract**

Novel tunnel FinFETs equipped with SiGe/Si heterojunction and multilayer fin-channel has been experimentally demonstrated. High quality SiGe layer is epitaxially grown on heavily doped Si source. SiGe/Si hetero-multilayer fin-channel with trigate configuration significantly enhances the drain current comparing with the conventional SiGe/Si heterojunction parallel-plate TFET.

## 1. Introduction

A tunnel field effect transistor (tunnel FET, TFET) is a candidate low power-consumption transistor for future "Internet of Thing" (IoT) application [1,2]. In order to increase the ON current and ON/OFF current ratio at small supply voltage, enhancement of tunnel probability for band-to-band tunnel (BTBT) transport and electric field applied at tunnel junction are important solutions to obtain sufficient performance [3-8].

In this paper, we experimentally demonstrate novel SiGe/Si heterojunction multilayer tunnel FinFETs. The SiGe has smaller band gap than Si and can increase tunnel probability. The SiGe/Si heterojunction is additionally introduced into tunnel FinFET structure with an epitaxial channel/source stack [4,7,9] which is effective to intensify the electric field at the tunnel junction. We evaluate the effectiveness of this novel architecture through device fabrication and TCAD simulation.

## 2. Experimental setup

**Figure 1** shows schematics of tunnel FinFETs. (a) is a conventional FinFET-like TFET with asymmetric source and drain polarity. (b) is a tunnel FinFET with ultrathin epitaxial channel layer, in which vertical BTBT is initiated between heavily doped source and undoped epitaxial channel [4,7,9]. Electric field applied to the epitaxial interface is intensified by synthetic electric field effect from both side- and top-gate electrodes. (c) is a novel heterojunction tunnel FinFET in the present study, which equips undoped SiGe epitaxial channel and "mille-feuille" type multilayer fin-channel, surrounded by gate electrode. **Figure 2** shows TCAD [10-12] simulated energy-band alignment of SiGe/Si parallel-plate (PP) stack. Reduction of energy band-gap of $Si_{0.7}Ge_{0.3}$ ($\Delta Eg = -0.19$ eV) at valence level in p-type tunnel-stack effectively shortens tunnel length enhancing BTBT probability at smaller bias voltage than homojunction tunnel-stack. However, as previously reported, BTBT in n-type SiGe/Si tunnel-stack cannot be enhanced compared to that of homojunction stack [6]. In the present study, we focus on the experimental evaluation of the p-type tunnel FinFET.

**Figure 3** shows process flow of the present SiGe tunnel FinFET. Source and drain regions were initially formed in the silicon-on-insulator (SOI) wafers by the ion implantation (I/I) technique. An ultra-thin SiGe and a Si cap-layers are epitaxially grown using vapor phase epitaxy. After the epitaxial growth, fin-patterning is performed. An $Al_2O_3$ gate insulator and a TiN gate electrode were deposited.

## 3. Results and discussion

**Figure 4** shows result of front-side secondary-ion mass spectroscopy (SIMS) analysis of SiGe heterojunction stack. Ge concentration is estimated up to 25%. **Figure 5** shows transmission electron microscopy (TEM) image of gate cross-section of fabricated TFET. Note that interface between n++ source well and SiGe interface has no interface defects. **Figure 6** shows measured transfer characteristics of SiGe/Si hetero-multilayer tunnel FinFETs compared with the parallel-plate TFETs with and without the SiGe/Si heterojunction. By introducing fin-channel, $I_{ON}$ increases significantly. However, OFF current is simultaneously deteriorated. In previous study, removal of SiGe layer on drain region significantly reduces $I_{OFF}$ of parallel-plate type SiGe TFET [6]. In the present case, such drain engineering is not adopted for the SiGe hetero-multilayer tunnel FinFET, and should be essential to realize both the enhanced $I_{ON}$ and ON/OFF current ratio simultaneously.

## 4. Summary

Novel tunnel FinFETs equipped with SiGe/Si heterojunction multilayer fin-channel are experimentally demonstrated. $I_{ON}$ enhancement by SiGe band-gap reduction and fin-channel is promising but $I_{OFF}$ suppression is also needed to realize sufficient ON/OFF ratio.

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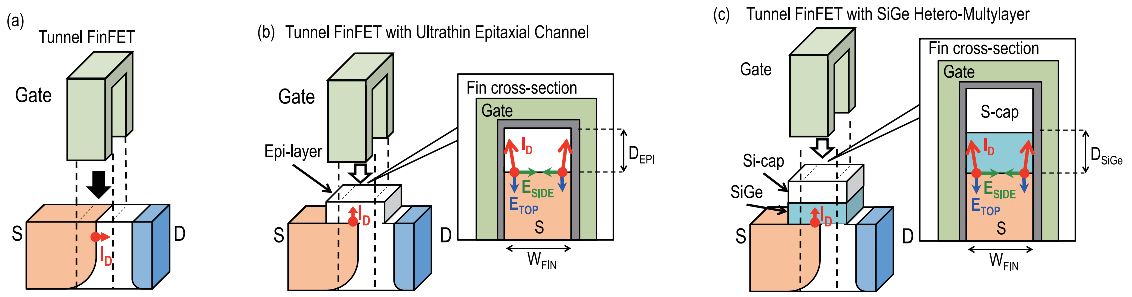


Fig. 1 Schematics of three types of tunnel FinFETs. (a) Conventional tunnel FinFET, which has asymmetric source/drain and 3-D trigate. (b) Tunnel FinFET with ultrathin epitaxial Si channel. Fin-patterning is performed after epitaxial growth. The outcroppings of source/channel interface are exposed at both side of the fin-channel. (c) Tunnel FinFET with SiGe channel, which has "mille-feuille" type multilayer fin-channel, surrounded by 3-D multigate electrode. The insets of (b) and (c) indicate synthetic electric fields applied at vertical tunnel junctions.

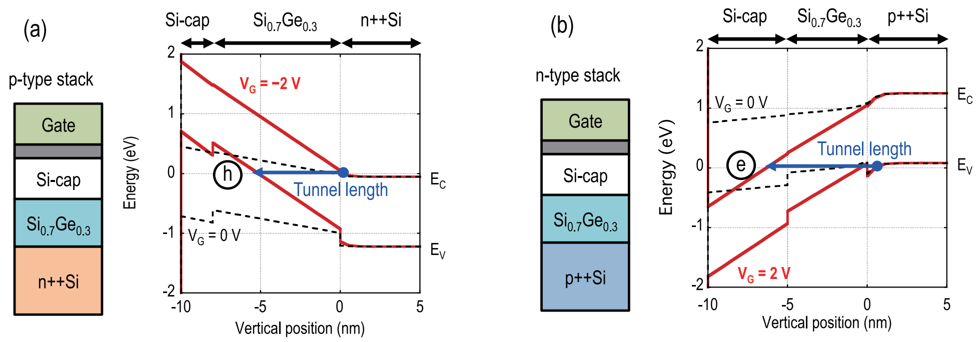


Fig. 2 Energy-bands of SiGe/Si heterojunction multilayer simulated by TCAD. Ge concentration is 30 % and $\Delta Eg$ = -0.19 eV. (a) p-type parallel-plate tunnel stack. Thicknesses of a Si-cap and SiGe layers are 2 and 8 nm, respectively. (b) n-type one. Thicknesses of both of Si-cap and SiGe layers are 5 nm. In (a), tunnel length is shortened by band-gap reduction in SiGe layer at valence energy level. However in (b), no tunnel length shortening is obvious.

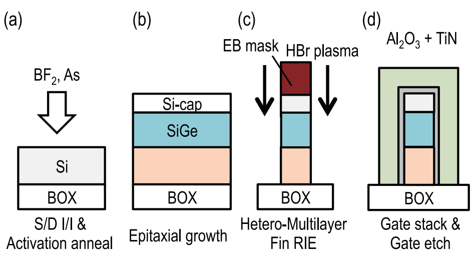


Fig. 3 Process flow of SiGe/Si hetero-multilayer tunnel FinFET.

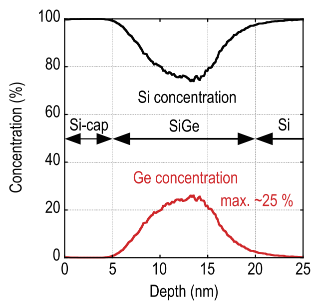


Fig. 4 Result of front-side SIMS analysis. Ge concentration in SiGe layer is estimated up to 25 %.

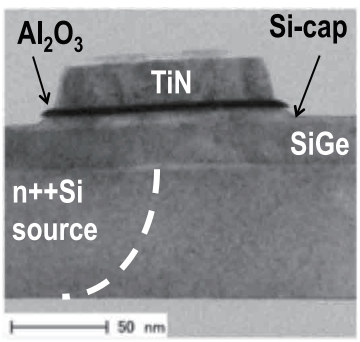


Fig. 5 TEM image of gate cross-section of fabricated TFET.

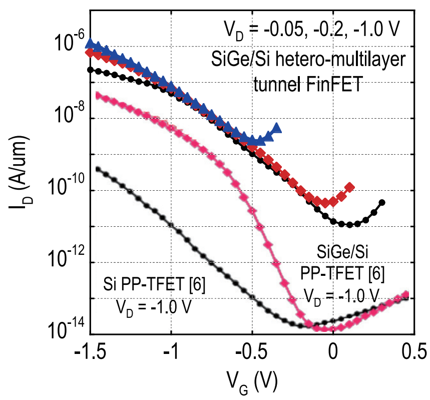


Fig. 6 $I_D$-$V_G$ characteristics of SiGe/Si hetero-multilayer tunnel FinFET. Those of planar parallel-plate TFETs with and without the SiGe/Si heterojunction are also indicated.