PS-1-3

Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp12-13

Improving performance of $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistors using *in situ* post remote-plasma treatment with N_2/H_2 gases

Quang-Ho Luc[1], Shou-Po Cheng[2], Jin-Han Chen[2], Guan-Yu Lin[3], Huy-Binh Do[1], Po-Chun Chang[2], Guo-Wei Huang[4], Kun-Ming Chen[4], Yueh-Chin Lin[1], and Edward Yi Chang[1, 2*]

[1] Department of Materials Science and Engineering, National Chiao Tung University
1001 University Road, Hsinchu 300, Taiwan
[2] Department of Electronics Engineering, National Chiao Tung University
1001 University Road, Hsinchu 300, Taiwan
[3]Institute of Imaging and Biomedical Photonics, National Chiao Tung University
1001 University Road, Hsinchu 300, Taiwan
[4]National Nano Device Laboratories, Hsinchu 30078, Taiwan
*E-mail: edc@mail.nctu.edu.tw

Abstract

We examine the impacts of post remote-plasma treatment with N_2/H_2 gases on the performance of the inversion-mode $In_{0.53}Ga_{0.47}As$ MOSFETs by employing *in-situ* atomic layer deposition process. Higher drain current, extrinsic transconductance, and effective electron mobility peak of $In_{0.53}Ga_{0.47}As$ MOSFET are obtained with good I_{ON}/I_{OFF} ratio and off state current. The enhancements on the performance of MOSFET devices treated with N_2/H_2 post remote-plasma are correlated with the effective passivation on the $In_{0.53}Ga_{0.47}As$ surfaces.

1. Introduction

In recent years, III-V compound semiconductors have attracted an extensive interest as a replacement for Si-based devices in future downscaling of complementary metal oxide semiconductor (CMOS) devices beyond 10 nm technology node. However, one of the major issues of high performance III-V based metal oxide semiconductor field effect transistors (MOSFET) is the inherently poor quality of high-k/III-V interfaces which degrades the gate controlability and the channel mobility [1]. In addition to many effors to passivate the III-V surfaces, post-gate plasma treatment with flourine (CF_4) has been proposed for realizing better interface quality of high-k/III-V [2]. In this work, an improved performance of $In_{0.53}Ga_{0.47}As$ nMOSFET has been demonstrated using post remote-plasma (PRP) treatment with N_2/H_2 gases after thermal-Al_2O_3 gate oxide as an *in situ* atomic layer deopostion (ALD) process. High drain current (I_{ON}), good subthreshold swing (SS), and better effective electron mobility peak (μ_{eff}) are achieved with N_2/H_2 PRP treatment. This approach, therefore, can provide an effective passivation for high performance InGaAs MOSFETs.

2. Experimental

Figure 1 shows the schematic cross section and fabrication process of a gate-first self-aligned $In_{0.53}Ga_{0.47}As$ nMOSFET. On p^+InP substrate, 100-nm p-doped 1×10^{18} cm^{-3} InP buffer layer and 50-nm p-doped 5×10^{16} cm^{-3} $In_{0.53}Ga_{0.47}As$ surface channel layer were sequentially grown by solid source molecular beam epitaxy. After degreasing in acetone and isopropanol, the native-oxides-covered samples were dipped in 4% HCl solution for 2 min followed by 10% $(NH_4)_2S$ solution for 20 min as pre-gate chemical treatment. Then, the samples were loaded into Atomic Layer Deposition (ALD) chamber (Cambridge NanoTech Fiji-202 DCS) for high-k deposition. In ALD chamber, trimethyl-aluminum (TMA) and water were used as precursors for Al_2O_3 film deposition. Chamber temperature was kept at 250°C during all processes. A 10-nm-thick Al_2O_3 layer was used as gate oxide (control sample). Some samples were treated by post remote-plasma N_2/H_2 (60/60 sccm flow rate) with plasma power of 150 W for 2 min. After that, post deposition annealing (PDA) was carried out at 450°C in 2 min in forming gas. A 100 nm-TiN metal gate electrode was deposited by physical vapor deposition. Gate pattern was defined via optical lithography and the TiN dry etching was conducted using inductively coupled plasma reactive ion etching (ICP-RIE). After source/drain (S/D) selectively implanted with silicon (Si), implantation activation was done by rapid thermal annealing (RTA) at 650°C for 15 sec in nitrogen (N_2). Au/Ge/Ni/Au S/D ohmic and AuBe backside contact were formed by e-beam evaporation. Finally, post metallization annealing (PMA) was performed at 270°C in 30 sec in N_2.

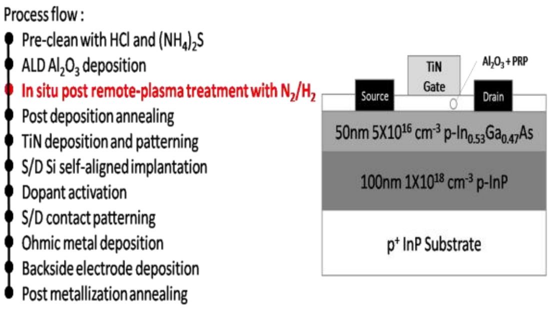

Fig. 1. Schematic cross section and fabrication process of a self-aligned inversion-mode n-$In_{0.53}Ga_{0.47}As$ MOSFET.

3. Results and discussion

Figure 2 shows the I_D-V_G characteristics of fabricated $In_{0.53}Ga_{0.47}As$ MOSFETs with gate length (L_G) of 6 μm and gate width (W_G) of 100 μm for samples with and without N_2/H_2 PRP treatment. Good subthreshold swing characteristics were observed for both samples with the on/off ratio of around 10^3. The subthreshold swing of sample with N_2/H_2 PRP treatment is improved from 195 mV/dec to 213 mV/dec as compared to control sample. Besides, the off state current is also suppressed with N_2/H_2 PRP treatment.

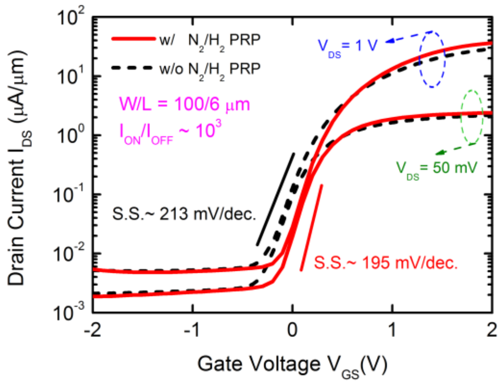

Fig. 2. I_D - V_G subthreshold swing characteristics of the $In_{0.53}Ga_{0.47}As$ gate-first self-aligned MOSFET with I_{on}/I_{off} ~ 10^3, L_G of 6 μm and W_G 100 μm with N_2/H_2 PRP treatment (red line) and without treatment (black-dash line).

The I_D-V_D characteristics of MOSFET with and without N_2/H_2 PRP treatment are shown in Fig. 3(a). The maximum drain current is 48.7 μA/μm ($V_{GS} - V_{Th}$ = 2 V and V_{DS} = 2 V) for N_2/H_2 PRP sample, increasing 60% as compare to 30 μA/μm of control sample. Figure 3(b) compares the drain current and extrinsic transconductance (G_m) as a function of gate voltage at 1 V of V_{DS}. The V_{Th} are 0.46 V and 0.44 V for control sample and N_2/H_2 PRP sample, respectively. The G_m maximum is increased from 20.38 μS/μm to 23.48 μS/μm for N_2/H_2 PRP sample. The improvements obtained with N_2/H_2 PRP treatment can be attributed to better interface quality of $Al_2O_3/In_{053}Ga_{0.47}As$. It is worth to pointing that nitrogen and hydrogen atoms are believed to allow perfect passivation on III-V surfaces.

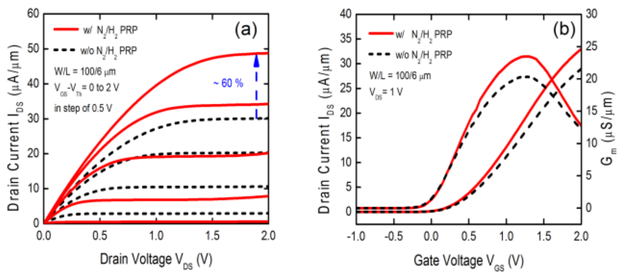

Fig. 3. (a) I_D – V_D characteristics as a function of V_{GS} - V_{Th} and (b) drain currents and extrinsic transconductance versus gate voltage of the $In_{0.53}Ga_{0.47}As$ MOSFETs with N_2/H_2 PRP treatment (red line) and without treatment (black-dash line).

Figure 4 shows the effective electron mobility (μ_{eff}) extracted from split CV method against surface carrier density (N_s). The peak mobility μ_{eff} of N_2/H_2 PRP sample is 3365 cm^2/Vs, 20 % higher than that of control sample (μ_{eff} of 2828 cm^2/ Vs).

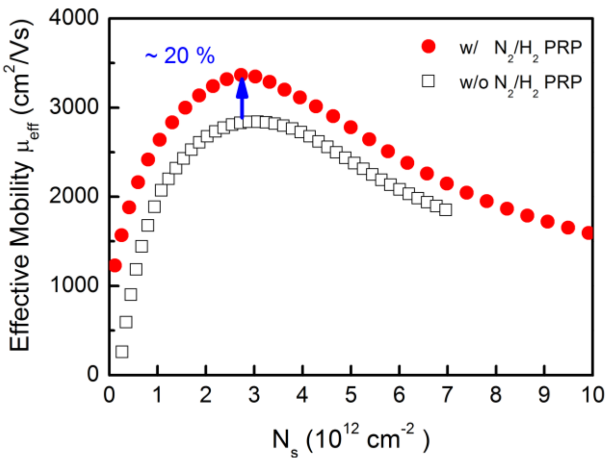

Fig. 4. The peak effective electron mobility (μ_{eff}) against inversion carrier density (N_s) of $In_{0.53}Ga_{0.47}As$ MOSFETs with N_2/H_2 PRP treatment (red circle) and without treatment (white square). .

4. Conclusions

In conclusions, the influence of *in situ* N_2/H_2 post remote-plasma treatment on the performances of $In_{0.53}Ga_{0.47}As$ nMOSFETs have been presented. By applying N_2/H_2 PRP treatment, the maximum drain current was improved by 60 % to 48.7 μA/μm while effective electron mobility peak was increased by 20 % to 3365 cm^2/Vs. The utilization of in situ post remote-plasma treatment can be favorable for better quality of high-k materials as well as interface of high-k/III-V, benefiting to performance of III-V based MOSFETs.

Acknowledgements

This work was sponsored by the NCTU-UCB I-RiCE program, Ministry of Science and Technology, Taiwan, under Grant No. MOST 104-2911-I-009-302.

References

[1] J. A. del Alamo, Nature **479** (2011) 317.

[2] Y. Wang *et al.*, Appl. Phys. Lett. **100** (2012) 243508.