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Sub-0.2V Switching Voltage of Negative Capacitance Double Gate Tunnel FET Using Ferroelectric Gate

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1. Introduction

To achieve the steep subthreshold slope transistors, the integration of tunneling transistor and negative capacitance (NC) would be an effective and possible solution [1]. Tunnel field-effect transistors (TFETs) bases on band-to-band tunneling (BTBT) operation to reach a steep subthreshold swing at subthreshold region [2-4]. Because of its small bandgap energy relative to Si, Ge could enhance the tunneling probability of TFET with high current requirements. Recently, epitaxially grown Ge (epi-Ge) p-TFETs on bulk (110) Si substrates [5] and planar p-TFETs on SOI (Si on insulator) [6] substrates have been reported. The hetero-tunnel field-effect transistor was proposed and modeled [7], demonstrating steeper switching and higher currents than conventional TFETs [8]. The concept of NC have great benefit to obtain body factor <1 to extend the steep slope region [9-12]. The NC-MOSFET structure using thin quantum well body, ie. Ultra-thin body (UTB), is calculated to suppress short-channel effects and sub-60mV/decade operation by modulation of MOS capacitance [13]. Therefore, the UTB Double gate (DG) TFET integrated with NC concept was performed in this work. The parameters of ferroelectric (FE) material thickness, body thickness and interfacial thickness is discussed for non-hysteretic behavior.

2. Concept and Devices Structure

The structure and band diagram of the UTB-DG-NC-TFET is designed as channel length (L_g) 40 nm (Fig. 1). The i-Si (n^--Si) is operated at accumulation region. The typical UTB-DG- TFET was calculated with Dynamic nonlocal path band-to- band model of TCAD for BTBT. The FE material is PZT (PbZrTiO3) with the parameters (Fig. 2 (a)) for FE calculation by Landau model [14]. The key to this design is the FE thickness to modulate C_{FE}, body thickness and interfacial thickness to adjust C_{MOS} (Fig. 3) according to voltage amplification ratio (Fig. 2(b)). Note C_{MOS} is calculated at accumulation region. The gain is following by the effective circuit of FE gate stack of UTB-DG (Fig. 2(c)).

3. Results and discussions

C_{FE} can be tuned by changing the FE thickness (T_{FE}). For FE=160nm, there are two cross points (A & B) between MOS and FE (Fig. 3), this is indicates hysteresis behavior due to $|C_{FE}|>C_{MOS}$. To obtain the maximum enhancement of voltage and non-hysteresis behavior due to NC effect, C_{FE} should be matched to C_{MOS} ($|C_{FE}|\sim C_{MOS}$) such as FE=153nm in this case (Fig. 3). Therefore, the corresponding transfer characteristics I_D-V_G shows the significantly improvement in SS and ON current (Fig. 4). Note that the T_{FE}=0nm indicates the control TFET without FE for reference. With NC effect, the SS_{min} is improved from 13 mV/dec to 8-5 mV/dec, and extended steep slope range (< 60mV/dec) from 8 orders to ~10 orders (Fig. 5). The T_{FE}=153nm presents the non-hysteresis and steeper slope with denoting as optimized condition. The extracted peak voltage amplification (A_V) of the optimized condition shows that ~ 35 (Fig. 6). In order to modulate C_{MOS}, the body thickness (T_s) is a critical factor and showing the body thin-down is beneficial for extending steep SS region (Fig. 7). Note that the T_{FE} is optimized thickness with steepest slope and non-hysteresis, ie. $C_{MOS} \sim |C_{FE}|$. The SS_{min} (~5 mV/dec) for ~ 5 order is obtained with T_s = 5 nm (Fig. 8). The corresponding amplification of NC effect shows almost the same (Fig. 9), and indicates not significantly different in optimized T_{FE} (Fig. 10). The interfacial layer thickness is another critical factor for discussion, and is set as SiO_2 in this work. The thin-down interfacial layer is beneficial for SS (Fig. 11), and showing SS_{min} ~ 6 mV/dec for 4 order with T_{ox} = 0.3 nm (Fig. 12). The negative shift in A_v peak with decreasing T_{OX} leads the steep slope in I_D-V_G (Fig. 13). Therefore, the optimized thickness of T_{FE} is decreasing with thinner T_{ox} (Fig. 14). This indicates the possible PZT thickness for CMOS process integration with extreme thin T_{ox} ~ 0.3nm for non-hysteresis. The Ge TFET is beneficial for BTBT due to small bandgap, therefore, Ge UTB-DG-NC-TFET is a candidate for sub-10nm technology with steep slope (SS_{ave} ~ 18 mV/dec), high ON current (> 100 μA/μm), and < 0.2V switching voltage (Fig. 15).

4. Conclusions

With optimizing T_{FE}, T_S, and T_{ox}, the Ge UTB-DG-NC-TFET exhibits steep slope (SS_{ave} ~ 18 mV/dec), high ON current (> 100 μA/μm), and < 0.2V switching voltage. The key concept of NC effect is C_{FE} matching to C_{MOS} ($|C_{FE}|\sim C_{MOS}$), and results smallest SS and non-hysteresis. The UTB-DG-NC-TFET is a candidate for sub-10nm technology in the future.

5. Acknowledgements

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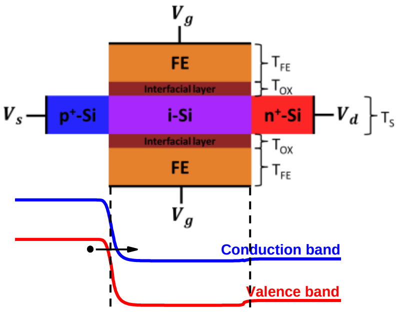


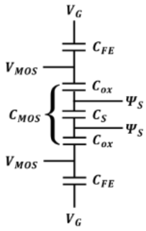
Fig. 1. The schematic diagram of UTB-DG-NC-TFET with Lg=40nm. T_{FE}, T_S, and T_{OX} are the thickness of ferroelectric material, body and interfacial layer, respectively.

	FE parameter
α	-4.89×10^{7} m/F
β	$4.76\times10^{7}\mathrm{m^5/C^2F}$
γ	$1.34\times10^{8}\mathrm{m^9/C^4F}$

(a)

$$A_v=\frac{\partial V_{MOS}}{\partial V_g}=\frac{|C_{FE}|}{|C_{FE}|-C_{MOS}}$$

(b)



(c)

Fig. 2. (a) The parameters of PZT as the FE material in this work. (b) The express of voltage amplification by NC effect. (c) The effective circuits of FE gate stack of UTB-DG.

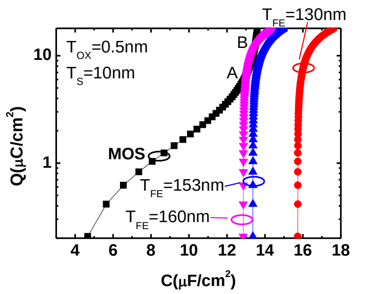


Fig. 3. The Q-C characteristics with different T_{FE}. The optimum condition is T_{FE}=153nm for minimum SS and non-hysteresis.

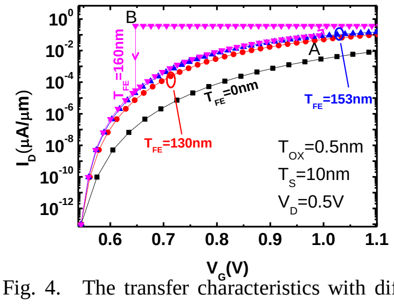


Fig. 4. The transfer characteristics with different T_{FE}. The hysteresis behavior is occurred with T_{FE}=160nm. Note that the T_{FE}=0nm indicates the control TFET without FE for reference.

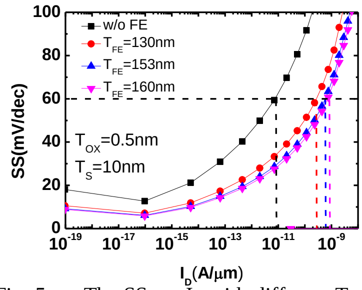


Fig. 5. The SS vs. I_D with different T_{FE}. The T_{FE}=153nm presents the non-hysteresis and steeper slope with denoting as optimized condition.

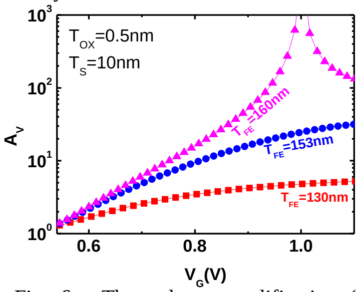


Fig. 6. The voltage amplification (A_v) with different T_{FE}. The extracted peak A_V of the optimized condition shows that ~ 35.

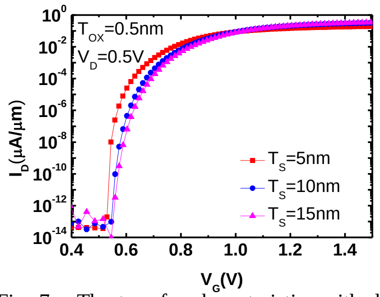


Fig. 7. The transfer characteristics with different T_s. The body thin-down is beneficial for extending steep SS region. Note that the T_{FE} is optimized thickness with steepest slope and non-hysteresis, ie. C_{MOS} ~ $|C_{FE}|$.

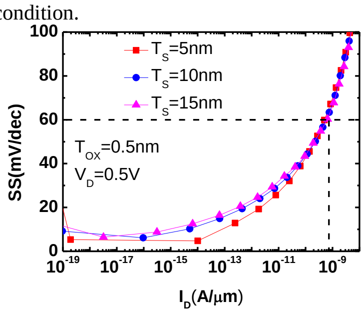


Fig. 8. The SS vs. I_D with different T_s. The SS_{min} (~ 5 mV/dec) for ~ 5 order is obtained with T_s = 5 nm

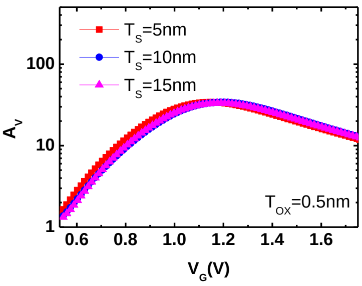


Fig. 9. The A_v with different T_s. The corresponding amplification of NC effect shows almost the same with different T_s.

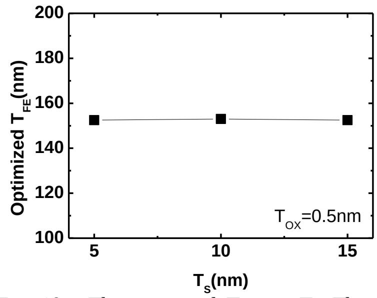


Fig. 10. The optimized T_{FE} vs. T_S. There is not significantly different in optimized T_{FE} with different T_S.

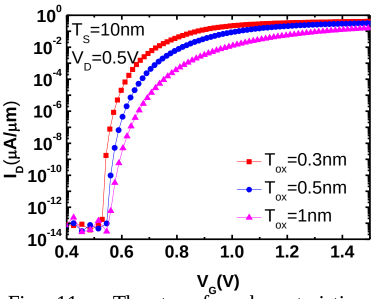


Fig. 11. The transfer characteristics with different T_{ox}. The thin-down interfacial layer is beneficial for SS.

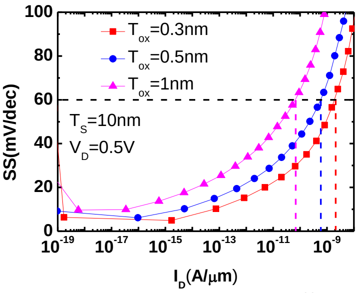


Fig. 12. The SS vs. I_D with different T_{ox}. It shows SS_{min} ~ 6 mV/dec for 4 order with T_{ox} = 0.3 nm.

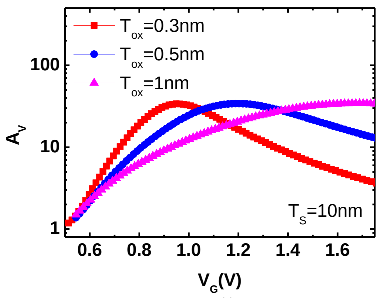


Fig. 13. The A_v with different T_{ox}. The negative shift in A_v peak with decreasing T_{OX} leads the steep slope in I_D-V_G

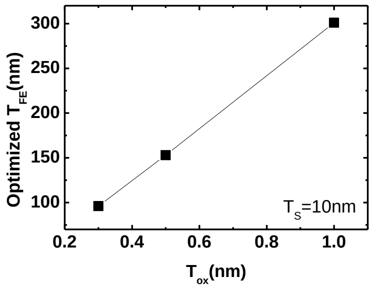


Fig. 14. The optimized T_{FE} vs T_{OX}. The optimized thickness of T_{FE} is decreasing with thinner T_{ox}. This indicates the possible PZT thickness for CMOS process integration with extreme thin T_{ox} ~ 0.3nm for non-hysteresis.

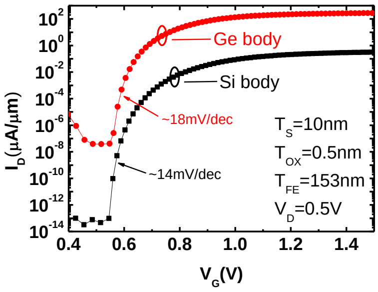


Fig. 15. The Ge TFET is beneficial for BTBT due to small bandgap, therefore, Ge UTB-DG-NC-TFET is a candidate for sub-10nm technology with steep slope (SS_{ave} ~ 18 mV/dec), high ON current (> 100 μA/μm), and < 0.2V switching voltage.