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Fabrication of Low-Temperature (< 400 °C) Germanium MOSCaps by Microwave Thermal Oxidation

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Abstract

We, for the first time, use microwave thermal oxidation (MTO) technique to form high quality gate dielectric on Ge at considerably low temperature (< 400 °C). In addition to grow GeO_2 interfacial layer, MTO was also employed for annealing after ALD Al_2O_3 deposition to effectively lower down the bulk trap density and interface trap density (D_{it}). With less than 400 °C, a D_{it} value of 8.68×10^{11} cm^{-2} eV^{-1} was achieved, which was ~54 % improvement as compared to the sample formed by conventional rapid thermal oxidation (RTO) at much higher temperature. Better reliability was also confirmed via constant field stress.

1. Introduction

Germanium has been regarded as one of the attractive material because of its higher electron (~3900 cm^2/V-s) and hole (~1900 cm^2/V-s) mobility than Si. However, high-κ/Ge interface quality is a key challenge due to the high value of D_{it}; GeO_2 grown by thermal oxidation is reported to be an appropriate passivation layer [1]. To further improve the interface quality, GeO_2 formed by low-temperature microwave thermal oxidation is an emerging technique to alleviate the interface roughness issue faced by other thermal approaches, e.g., RTO. In this work, we firstly demonstrate forming high quality $Al/Al_2O_3/GeO_2$/p-Ge MOSCaps below 400 °C with the help of MTO. We find that the D_{it} can be improved effectively by this novel technique as compared to the RTO.

2. Experiment

(100)-oriented p-type Ge substrate with resistivity 0.01~0.05 Ω-cm was used for fabricating MOSCaps. First, the samples were cleaned by diluted hydrofluoric acid and DI water (DHF: H_2O = 1:20) to remove the native oxide. We used two schemes to form the GeO_2 layer. The GeO_2 in the MTO case was formed by 2.4 kW microwave oxidation for 30 s; while that in the RTO case was formed by the conventional rapid thermal oxidation at 450 °C for 10 s. The temperature profile of microwave-activated anneal is shown in **Fig. 1**. We found the T_{peak} for MTO was of ~360 °C which was much lower than that for RTO. Sequentially, we deposited a 5 nm-thick Al_2O_3 by atomic layer deposition at 250 °C. In order to improve the quality of gate dielectric stack, we then used second thermal treatment and named them as DMTO (double MTO) and DRTO (double RTO). DMTO was formed by adding a 100 s 1.6 kW microwave anneal in O_2 ambient after Al_2O_3 deposition, which T_{peak} ~380 °C, as shown in **Fig. 1**. Contrast to DMTO, DRTO was made by performing another 450 °C rapid thermal anneal in O_2 ambient for 30 s. Next, a 300 nm-thick Al film was deposited by physical vapor deposition (PVD) and patterned by photolithography as the gate electrodes. Finally, Ti (5nm)/Al (300 nm) was deposited by PVD for the backside contact. Process flow and schematic structure are shown in **Fig 2**.

3. Results and Discussion

Figs. 3(a) and **(b)** show the TEM images of $Al/Al_2O_3/GeO_2$/p-Ge gate stack with GeO_2 grown by MTO and RTO. **Figs. 4(a)**, **(b)**, **(c)** and **(d)** show the multi-frequency C-V characteristics of $Al/Al_2O_3/GeO_2$/Ge MOSCaps with RTO only, DRTO, MTO only and DMTO, respectively. DMTO depicted the steepest C-V curve and the least hump in the depletion and weak inversion regions than the other cases, revealing that the value of D_{it} was effectively reduced. Furthermore, its C_{ox} value was slightly higher and V_{FB} lower than those of MTO, as shown in **Table I**, which could be attributed to the reduction of slow traps and fixed charges in the high-κ dielectric. For specifying the D_{it} value, we used the conductance method. **Fig. 5** shows the extracted D_{it} distribution versus energy near the midgap at room temperature for four cases. Both MTO and RTO had the D_{it} value of around 1.85×10^{12} cm^{-2} eV^{-1} at the energy level of 0.235 eV. However, the value of D_{it} was significantly reduced by 54% with using DMTO; while only 37% improvement was obtained by DRTO. We think that this might be explained by the specific and non-thermal microwave effect [2-3]. Microwave can supply the localized phonon excitation through resonant coupling to weak surface bonds efficiently. This mechanism can be used to repair the dangling bonds or weak bonds of the interface between GeO_2/Ge. Based on the microwave induced resonant coupling, the D_{it} value can be significantly reduced to around 8.68×10^{11} cm^{-2} eV^{-1} by employing additional MTO treatment.

Figs. 6(a) and (b) show the shifts of high frequency C-V curve for DRTO and DMTO under the constant field FN stress. DRTO exhibited obvious V_{FB} shift induced by positive bias stressing but DMTO only showed slight shift. This means DMTO has better immunity against stress than DRTO and is believed to be closely related to the reduction of bulk trap density of the dielectric stack.

3. Conclusions

We firstly demonstrate the formation of $Al/Al_2O_3/GeO_2$/p-Ge MOSCaps with low-temperature microwave-activated thermal process. With proper scheme, the D_{it} value of around 8.68×10^{11} cm^{-2} eV^{-1} can be achieved by using DMTO. As compared to the conventional RTO technique, we can form the dielectric stack with better quality by MTO at much lower temperature in terms of D_{it} and reliability.

Acknowledgements

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References

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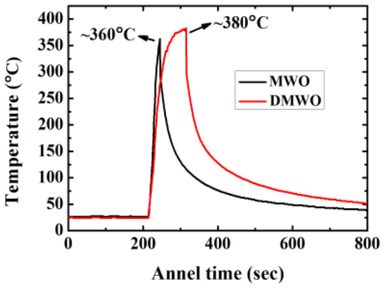

Fig. 1 Temperature (°C) versus anneal time for MTO and DMTO.

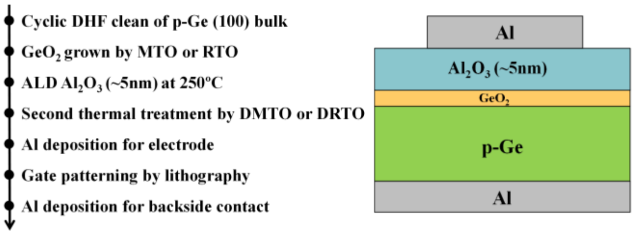

Fig. 2 Process flow and schematic structure of Al/ Al_2O_3/GeO_2/p-Ge MOSCaps.

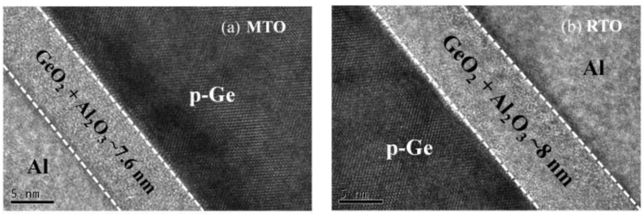

Fig. 3 TEM images of $Al/Al_2O_3/GeO_2$/p-Ge gate stack with GeO_2 grown by (a) MTO (b) RTO.

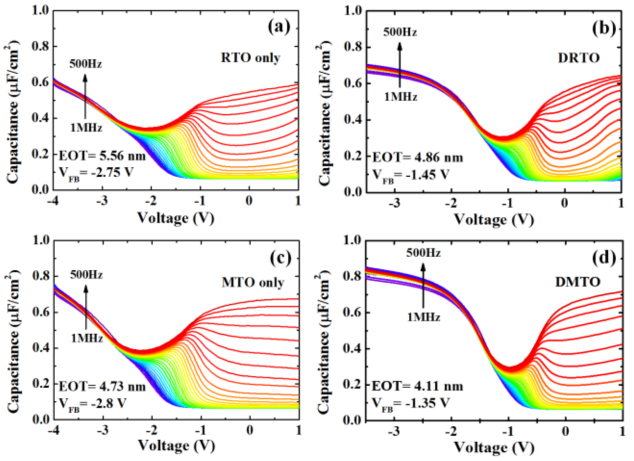

Fig. 4 C-V characteristics of $Al/Al_2O_3/GeO_2$/p-Ge MOSCaps with GeO_2 grown by (a) RTO only (b) DRTO (c) MTO only (d) DMTO respectively.

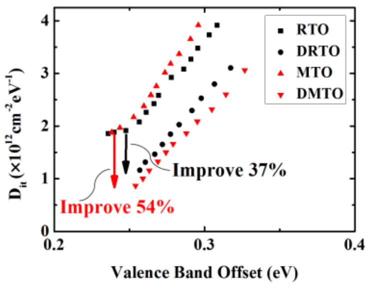

Fig. 5 D_{it} distribution of RTO, DRTO, MTO and DMTO MOSCaps.

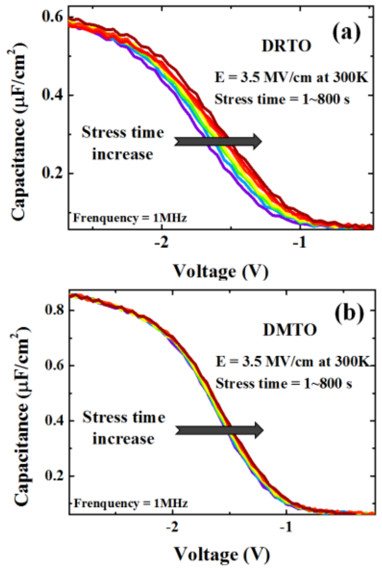

Fig. 6 C-V characteristics of $Al/Al_2O_3/GeO_2$/p-Ge MOSCaps under constant field FN stress for (a) DRTO and (b) DMTO cases.

	C_{ox} ($\mu F/cm^2$)	EOT (nm)	V_{FB} (V)	D_{it} (cm^{-2} eV^{-1})
RTO	0.62	5.56	-2.75	1.85×10^{12}
MTO	0.73	4.73	-2.8	1.88×10^{12}
DRTO	0.71	4.86	-1.45	1.16×10^{12}
DMTO	0.84	4.11	-1.35	8.68×10^{11}

Table I Summary of key capacitor parameters.