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Top-Gated Epitaxial Bilayer $MoSe_2$ Transistors on AlN Wafers & The Impact of Top-Down Process-Induced Damage

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Abstract

We report for the first time channel-patterned top-gated field-effect transfer characteristics of large-area epitaxial $MoSe_2$ bilayers transistors on AlN substrates. Current modulation up to 100 times is observed for a large number of devices. We show that top-down channel and gate patterning can have pronounced impact on the electronic behavior of these ultra-thin channel devices.

1. Introduction

Over the years, transistor scaling has relied on clever solutions to enhance device performance, such as novel high-k dielectrics. To achieve precise electrostatic gate control, ultrathin oxides are needed culminating in large leakage currents and device degradation. Nowadays, large area of bidimensional transition metal dichalcogenides monolayer can be obtained, allowing better gate control over the channel barrier with reduced short-channel effects [1]. Recently, manufacturability of these layered materials has gained a large momentum but yet important elements in the process integration are not developed. Here, we focus on develop top-gate transistors in which the channel is patterned down to 500 nm widths and are made of large-area epitaxial $MoSe_2$ grown on AlN substrates.

2. Bilayer $MoSe_2$ field-effect transistors

Material Growth and Raman Characterization

A target thickness of two monolayers of large-area $MoSe_2$ are epitaxially grown in a UHV-MBE chamber on a template AlN seed layer. The hexagonal AlN 200-nm thick seed layer is deposited by metalorganic chemical vapor deposition (MOCVD) on B-doped p-type 200 mm Si(111) substrates. A comprehensive study on the epitaxial growth and physical characterization of the $MoSe_2$ layers used in this work has been reported elsewhere [2]. The layers are crystalline on top of the AlN and are continuous across a 2-inch wafer. To verify the stability of the layers when exposed to ambient conditions, Raman and photoluminescence (not shown) spectra have been recorded across the wafer at different days after first exposure to air, and are depicted in Fig. 1(a).

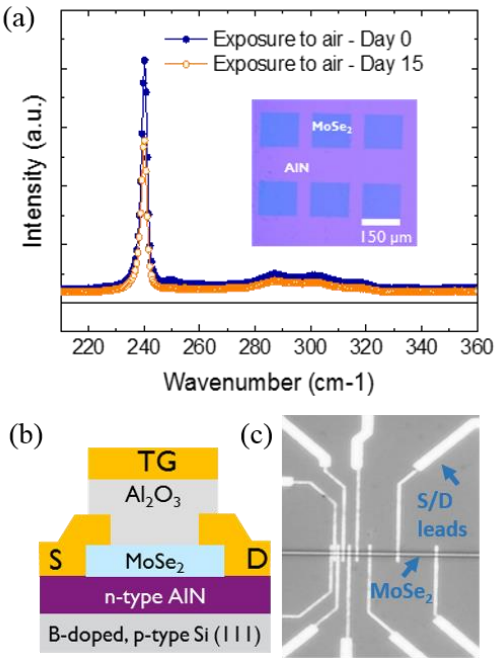

Fig. 1 (a) Bilayer $MoSe_2$ Raman spectra measured at different times after air exposure. (inset) Optical microscope image of large patterned areas of $MoSe_2$ on AlN. (b) Schematic cross section of a top-gated bilayer $MoSe_2$ transistor (c) Optical image of a TLM structure without top-gate for clarity. Both channel and contact widths are 500 nm.

The characteristic A1g peak sitting at 240.2 cm^{-1} corresponds to a bilayer of uncapped $MoSe_2$ with a strong, and expected, photoluminescence at 800 nm. After two weeks, the spectra are recorded again and no peak shifts are observed, except for a slight intensity reduction. This remarkable stability can be attributed to the low reactivity of Se [3] and possible vacancy passivation at the $MoSe_2$-AlN interface. The inset in Fig. 1(a) shows an optical micrograph of uninterrupted 150x150 um^2 $MoSe_2$ (blue) squares patterned on the AlN (magenta) substrate.

Device Integration

The schematic of top-gated field effect transistors used in this study is illustrated in Fig.1(b). The major achievement of this work was the development of a novel channel-patterning integration scheme with significantly high device yield. Figure 1(c) shows top-down optical microscope device image prior to top-gate patterning for clear visualization of the patterned channel. Channels widths varying from 500 nm to 2 µm and fixed length of 5 µm were patterned with electron beam lithography (EBL) exposed on a 120-nm thick hydrogen silsesquioxane (HSQ) negative-tone hard mask layer. The pattern was transferred to the $MoSe_2$ by a low-power Ar milling step. The remaining hard mask material was removed by immersion in a buffered hydrofluoric (BHF) acid solution. The AlN insulating substrate is insensitive to the hard-mask patterning and BHF treatment and no substrate damage was observed, in agreement with Ref. [3]. Source and drain contacts were fabricated via an additional EBL step, followed by e-beam metal evaporation of Ti (0.5 nm)/Pd (50 nm). Subsequently, 15 nm of Al_2O_3 was deposited via atomic layer deposition at 450 K and with an additional EBL to define the top gate followed by Ti (5 nm)/Au (60 nm) metallization.

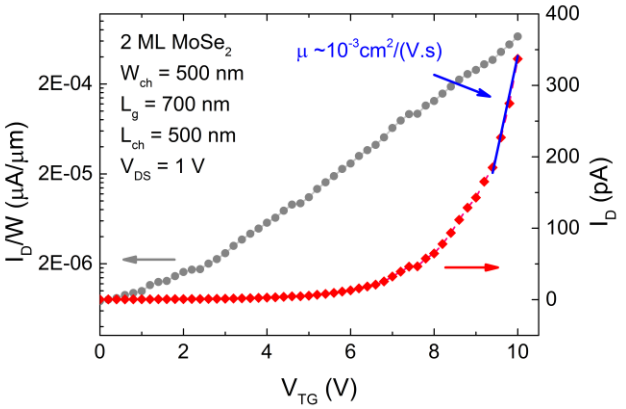

Fig. 2 Room-temperature transfer characteristics for a $MoSe_2$ bilayer top-gate transistor showing current modulation of about 100 times. Right axis values plotted on linear scale

Electrical characterization

Top-gated transfer characteristics for a bilayer transistor with a 500-nm wide channel is shown in Fig. 2. Source-drain bias voltage is 1V and the overlapping (~ 100 nm) top-gate is swept between -10 to 10 V. Note this is the first time top-gate modulation is observed for synthetic $MoSe_2$-based transistors with patterned channels. Most of the work reported in literature is for as-grown synthetic materials without any channel patterning. However, channel patterning is an important component towards technological applications. As previously mentioned, the device yield with this novel integration flow is of about 80% and we have measured more than 40 devices with similar conduction characteristics. Current modulation is about 100 times and the limited device performance is assumed to be originated from processing-induced damage introduced to the channel during the patterning process. This can be an additional reason why our devices suffer from high contact resistance (~160 kΩ.µm at zero bias), besides un-optimized contact metal work-function. The high resistance prevents the device from reaching current saturation. Field-effect mobility is estimated close to gate leakage threshold bias from the sheet resistance, assuming parallel plate gate capacitance and is in the order of 10^{-3} $cm^2/(V.s)$. The mobility value is an estimate and not perfectly accurate. This allows us to conclude that in order to further boost device performance, improvement in channel-patterning is certainly a key challenged to be addressed for 2D transistor technologies.

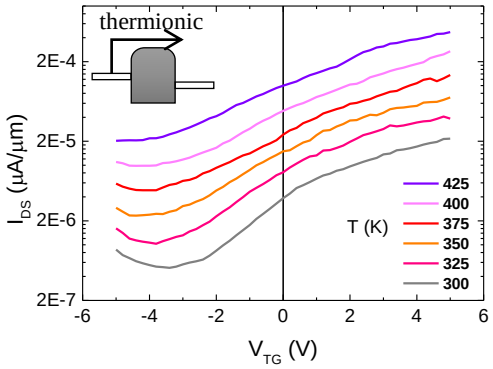

Fig. 3 Temperature-dependent transfer characteristics for the same device as in Fig. 2.

We investigate temperature-dependent conduction (Fig. 3) for the same device reported in Fig. 2. Thermionic emission seems to be the main transport mechanism but low-temperature measurements need to be carried out to assess if the diffusive conduction is present and also to determine possible tunneling properties.

3. Conclusions

We report top-gated transport characteristics for a bilayer epitaxial large-area $MoSe_2$ transistor with patterned channel on AlN substrate. Estimated mobility is low and we believe process-induced damage is the main reason for deterioration of high-performance conduction, stating a clear need for innovative channel-patterning schemes for reaching high-performance 2D-based devices.

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References

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