Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp444-445

$Al_2O_3/HfO_2/Al_2O_3$/Graphene Charge Trap Flash Device with a Self-aligned Gate

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Abstract

Graphene-based nonvolatile memory (GNVM) has a large memory window. As the scale of GNVM is reduced, the ratio of access resistance R_A to total channel resistance R_{TOT} is increased. To investigate the influence of this change, we fabricated GNVMs with various access lengths and self-aligned structure. Our self-aligned structure minimizes the access length, and thereby improves the drain current, on/off current ratio and electrical characteristics of GNVM. The off-current of the self-aligned GNVM is increased from 0.16 mA to 0.28 mA because R_{TOT} is reduced, but the on-current is also increased from 0.35 mA to 0.72 mA, so the on/off ratio is increased from 2.18 to 2.57.

1. Introduction

Graphene-based electronic devices candidates to replace silicon-based electronics. Graphene has very high theoretical carrier mobility, $\mu = 200{,}000\ cm^2 \cdot V^{-1} \cdot s^{-1}$, compared to silicon.[1, 2] In addition, a graphene channel is transparent and flexible, so it can be applied to future devices such as high-frequency applications, wearable devices and flexible devices.[4] GNVM is one of the most attractive parts of graphene-based electronics. Generally, GNVM has an ambipolar conduction property, so its memory window is twice as large as that of conventional CMOS memory device. We propose a self-aligned GNVM with HfO_2 as a charge trap layer, and Al_2O_3 as both tunnel oxide and block oxide.[3, 6] As graphene devices are scaled down, the channel resistance R_C under the gated region becomes comparable to the access resistance R_A between the source/drain contacts and the gated graphene channel (GC), so drain current I_D decreases.[5] In addition, reduced I_D make the device performance degrade, so self-alignment is essential in downscaling of the device. To identify the effect of self-alignment, we compare self-aligned GNVM with non-self-aligned GNVM.

2. Fabrication method

First, the single-layer graphene grown on Cupper film by CVD (chemical vapor deposition) is transferred onto a SiO_2 (100nm)/n-type Si substrate. We used Raman spectroscopy to confirm the quality of graphene and to determine whether or not it is in single-layer form. Second, to pattern the GC area, an ultrathin Al layer (1nm) is deposited on the graphene and naturally oxidized in air. Next, Al_2O_3 (7 nm) as a tunnel oxide was deposited on the naturally-oxidized

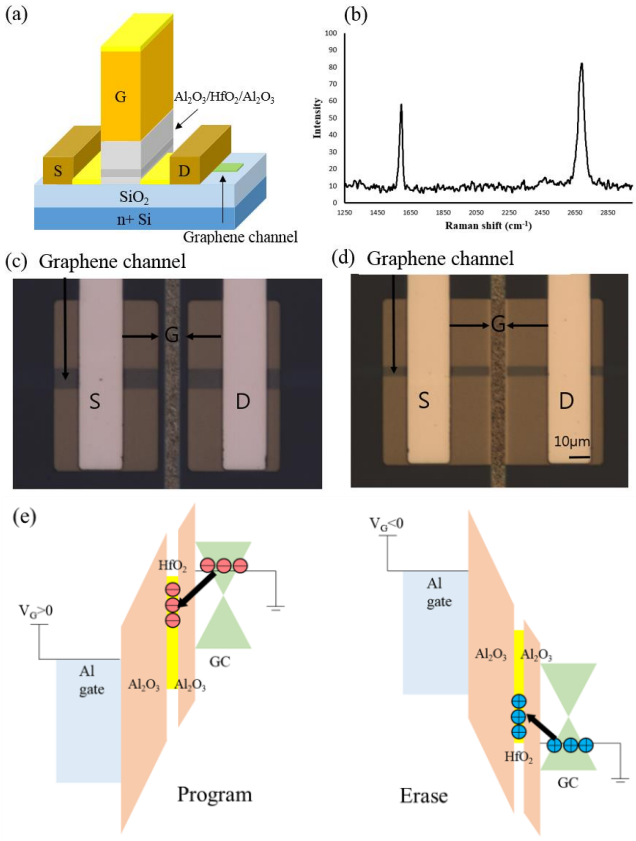

Figure 1. (a) Schematic illustration of graphene charge trap memory device with a self-aligned gate. (b) Raman spectrum of graphene channel. Optical microscope image of (c) non-self-aligned structure with L_A = 2 μm and (d) self-aligned structure. (e) Two band diagrams of GNVM across the gate stack. (Left: $V_G = V_{P/E} > 0$, Right: $V_G = V_{P/E} < 0$)

thin Al_2O_3 layer.[7] This tunnel oxide was patterned by photolithography and etched using 1000:1 DHF solution, then the exposed graphene was etched using oxygen plasma to define the GC.[8] In most cases of graphene device, photoresist residues degrade μ of the GC.[9] However, the tunnel oxide layer can prevent the GC from photoresist. Then, HfO_2/Al_2O_3 (7 nm/35 nm) layers were subsequently deposited by atomic-layer deposition, and an Al gate electrode (300 nm) was formed by e-beam evaporation and lift-off. In addition, the triple stack of the $Al_2O_3/HfO_2/Al_2O_3$ (7 nm/7 nm/35 nm) was etched using hybrid etching. If only wet etching is used (to protect the graphene), self-alignment is impossible due to its isotropic characteristic. However, if only dry etching is used, the GC is damaged. The

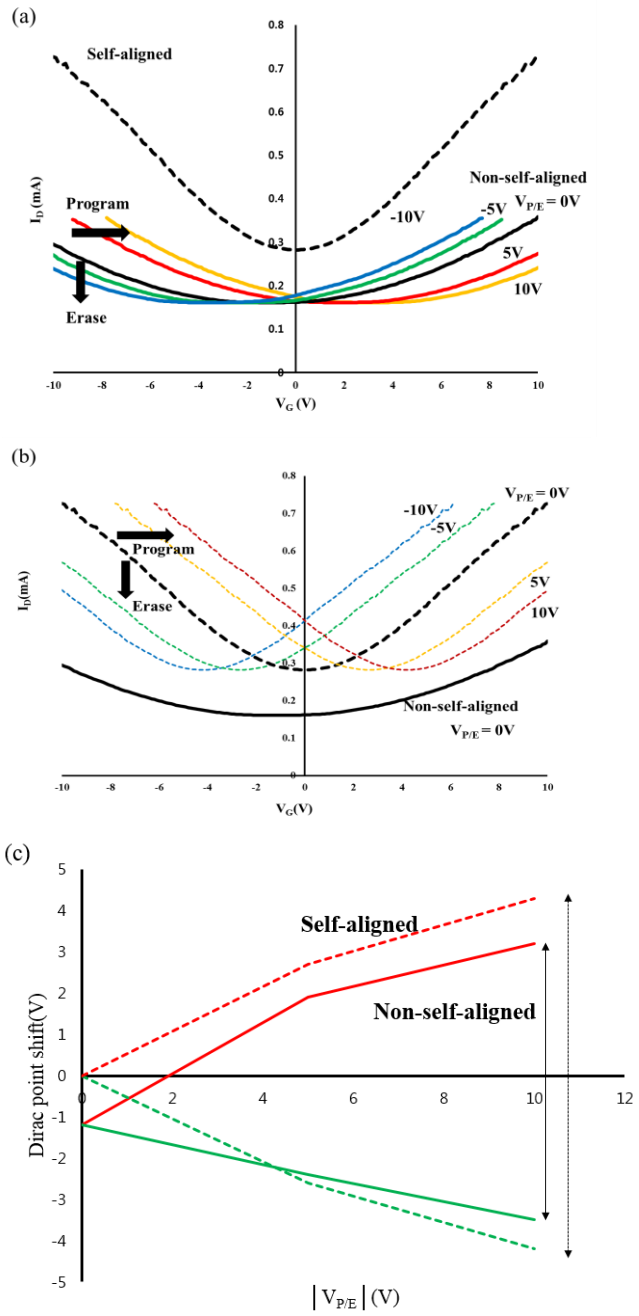

Figure 2. I_D-V_G characteristic curves (V_D=1V) of a non-self-aligned GNVM (a) and a self-aligned GNVM (b) at various $V_{P/E}$ ($V_{P/E}$ = -10V, $V_{P/E}$ = -5V, $V_{P/E}$ = -0V, $V_{P/E}$ = 5V, $V_{P/E}$ = 10V). (c) Variation of the Dirac point shift as a function of $V_{P/E}$. (bold line: non-self-aligned, dashed line: self-aligned)

HfO_2/Al_2O_3 (7 nm/35 nm) layer was etched using an inductively coupled plasma (ICP) etcher using the gate electrode as a hard mask; the other Al_2O_3 (7 nm) layer which provides an etch stop layer was etched using 1000:1 HF solution. The isotropic etch characteristic of the wet etch process allows a T-shaped gate stack to form naturally, and is crucial to achieve self-aligned gates without any sidewalls. Then, shallow source/drain electrodes (10 nm) were aligned by the edges of the gate. Finally thick source/drain metal pads (300 nm) were formed by e-beam evaporation and lift-off.

3. Result and Discussion

To compare self-aligned GNVM with non-self-aligned one, we fabricate self-aligned GNVMs and non-self-aligned GNVMs which have the access length L_A=2μm. Self-aligned GNVM has a slightly larger memory window (MW) than non-self-aligned GNVM. The Dirac point shift ΔV_{Dirac} of the GC is determined by the trapped charge in HfO_2, so the size of MW is independent of the self-alignment, but the high current on/off ratio can measure ΔV_{Dirac} precisely. The devices with self-aligned GNVM had higher I_D, and higher on current (0.72 mA, Figure 2) than did devices with non-self-aligned GNVM (0.35mA, Figure 2). Devices with self-aligned GNVM had higher on/off ratio (2.57) than devices with the non-self-aligned GNVM (2.18) to 2.57. However, devices with the self-aligned GNVM had higher off current (0.28 mA) than did devices with non-self-aligned GNVM (1.6 mA) because self-alignment minimizes the total resistance of the GC.

4. Conclusions

We introduce a GNVM that has self-aligned structure, and investigate its influences on some electrical characteristics of the GNVM. The self-aligned structure can minimize contamination of the graphene-based electronic devices by photoresist during fabrication. The self-aligned structure is also essential for scaling down the devices, and can improve the electrical characteristics of the GNVM by reducing R_A.

Acknowledgements

The authors thank the graphene-research group under Advanced Nano Device Laboratory (ANDLAB) in POSTECH. This work is supported by Samsung electronics through the Samsung POSTECH Research Cooperation (SPRC) program. The fabrication process is supported by National Institute for Nanomaterials and Technology (NINT) in POSTECH.

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