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Characterization of Near-Interface Oxide Trap Density in SiC MOS Capacitors by Transient Capacitance Measurements at Various Temperatures

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Abstract

Near-interface oxide trap density in SiC MOS capacitors was estimated by transient capacitance measurements at room- and low- temperatures. We found that the sample which had better *C-V* characteristics showed smaller density of near-interface traps especially in spatially shallow region in the oxide.

1. Introduction

SiC MOS capacitors with thermal oxides are often severely suffered from near-interface oxide traps [1], but the method to quantitate those traps has not been established well. We have already proposed a method to estimate them from transient capacitance (*C-t*) characteristics [2]. This method assumes the model that carriers in semiconductors interact with the traps in oxide by tunneling [3], thus response time of the traps is widely spread due to the variation of the tunneling distance between the interface and the traps. However, the one of the challenging issues of this method has been the limitation of the detectable trap distance from the interface, *i.e.* the response time of spatially shallow traps is too short to detect with conventional *C-t* measurement system. In this study, we employ low temperature *C-t* measurements to characterize those shallow traps.

2. Analysis of Transient Capacitance Response

From *C-t* characteristics, we can estimate the amount of traps, as well as their response time since the surface potential of MOS capacitors will change with de-trapping of oxide traps. The gate bias on capacitors was kept in accumulation state ($V_g = V_{trap}$) for 100 s to fill the traps, before a sudden shift to the near-flatband state ($V_g = V_{meas}$) to observe *C-t* characteristics. Taking into account of the widely-spread time constants of the traps due to their depth distribution in oxide, the time-dependent change of capacitance (ΔC) would be described by "extended-Debye relaxation model" [2, 4], instead of a conventional relaxation model with a single time constant. When a voltage bias on capacitor suddenly shifts to V_{meas} at $t = 0$, ΔC is expected to be described by,

$$\Delta C \equiv \left|C(t) - C_{eq}\right| \cong \left|\Delta C_0\right| \exp\left[-\left(\frac{t}{\tau_{eff}}\right)^{\beta}\right] \qquad (1)$$

where C_{eq} is the capacitance in thermal equilibrium, β is the stretched exponential factor ($0 < \beta < 1$) of the response time, τ_{eff} is the effective response time of the group of traps with distributed response time, and ΔC_0 is the total change of capacitance caused by the trapped charges. We fit those parameters of this equation to the measured curve to determine the amount of trapped charges per area in near-interface oxide (Q_{ox}), followed by the estimation of state density of oxide traps (D_{ox}) by,

$$D_{ox} \cong \frac{1}{q}\frac{dQ_{ox}}{d\varphi_s} \qquad (2)$$

where φ_s is the surface potential corresponding to V_{trap}. We assume that carrier response time τ is determined by the transport in oxide by tunneling, thus τ is written [5] by

$$\tau(x,T) = F(E,T)\,\tau_0(E)e^{2\kappa x} \qquad (3)$$

where x is tunneling distance in oxide, τ_0 is time constant of the interface traps which weakly depends on T, κ is the attenuation coefficient for an electron wave function of energy E, and F is Fermi-Dirac function which strongly depends on T. Because Fermi-Dirac function becomes more precipitous at lower temperature, τ at 200 K is a few orders larger than that of room temperature. Thus low temperature measurements enable us to detect the shallow traps even by a conventional system, which were difficult to detect at room temperature, as schematically shown in **Fig. 1**.

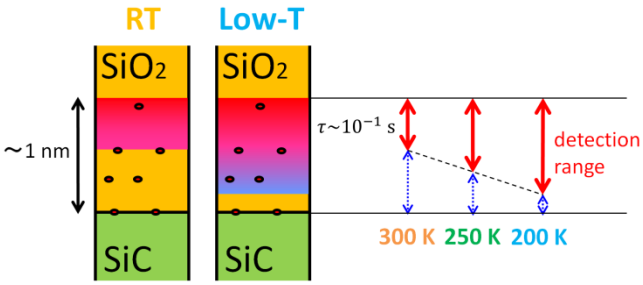

Fig. 1 Schematic of oxide trap detection range of spatial distance from SiO_2/SiC interface at various temperatures. The distance from the interface indicated in the figure is approximately estimated by taking account of the tunneling mass of electrons and eq.(3).

3. Fabrication of 4H-SiC MOS Capacitors

MOS capacitors A and B were fabricated on 4H-SiC wafers with ~1×10^{16} cm^{-3} doped n-type epitaxial layers, by thermal oxidation at 1300°C in dry-O_2. In spite of the nominally identical processes they showed different characteristics because of uncontrollable experimental factors. The oxide thicknesses were ~14 nm in common.

4. Results and Discussions

Bidirectional *C-V* characteristics of sample A and B are shown in **Fig. 2**. Interface state density (D_{it}) of sample

A at $E_c - E \sim 0.2$ eV was $\sim 10^{11}$ cm^{-2}eV^{-1} whereas that of sample B was $\sim 10^{12}$ cm^{-2}eV^{-1}. Additionally, sample B shows hysteresis indicating the existence of non-negligible amount of near-interface traps.

The typical *C-t* characteristics of sample B obtained for different V_{trap} and for different temperatures are shown in **Fig. 3 (a)** and **(b)**, respectively. Data for each sample were well fitted by eq. (1) as shown in **Fig. 3 (a)**. From **Fig. 3 (b)**, response time of detected carrier tunneling was shorter and ΔC_0 was larger at low temperature suggesting high density of shallow traps. Note that difference of τ_{eff} is not directly corresponded to the difference of tunneling distance because the response time is a strong function of temperature as indicated by eq. (3). To compensate the effects of temperature, $\tau_{\mathrm{eff}}/F(E,T)$ was considered as an indicator of the tunneling distance, and shown in **Fig. 4**. It is clearly seen that data are separated into two regions, which means that there are two groups of oxide traps that exist in spatially shallow region and deep region, respectively.

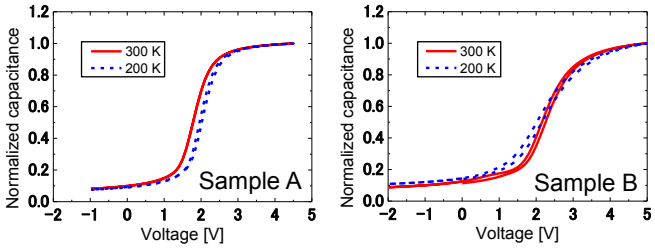

Fig. 2 1 MHz bidirectional *C-V* characteristics of two kinds of SiC MOS capacitors A and B.

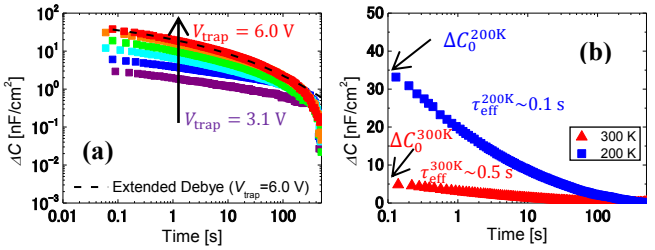

Fig. 3 *C-t* characteristics of sample B, (a) with various V_{trap} at 200 K, and (b) at different temperatures with V_{trap} = 6.0 V.

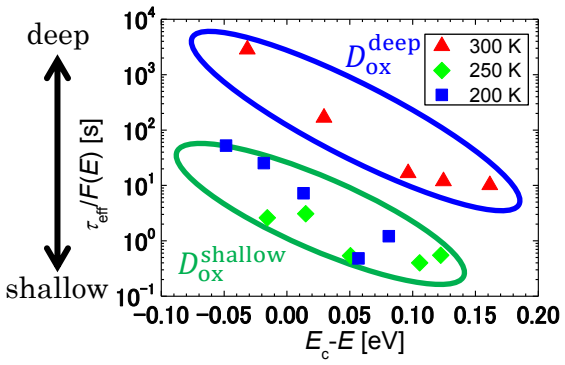

Fig. 4 Energy dependence of effective response time τ_{eff} divided by Fermi-Dirac distribution function $F(E,T)$.

Fig. 5 (a) and **(b)** show the oxide trap state density of spatially shallow traps ($D_{\mathrm{ox}}^{\mathrm{shallow}}$) and deep traps ($D_{\mathrm{ox}}^{\mathrm{deep}}$), respectively. For sample A, $D_{\mathrm{ox}}^{\mathrm{shallow}}$ was approximately one order smaller than the one for sample B. On the other hand, there was no remarkable difference in $D_{\mathrm{ox}}^{\mathrm{deep}}$. These results suggest that the density of oxide traps in the shallow region, estimated to locate only a few Å from the interface by assuming a tunneling mass of electrons [6] in eq.(3), is quite sensitive to a slight difference of process conditions.

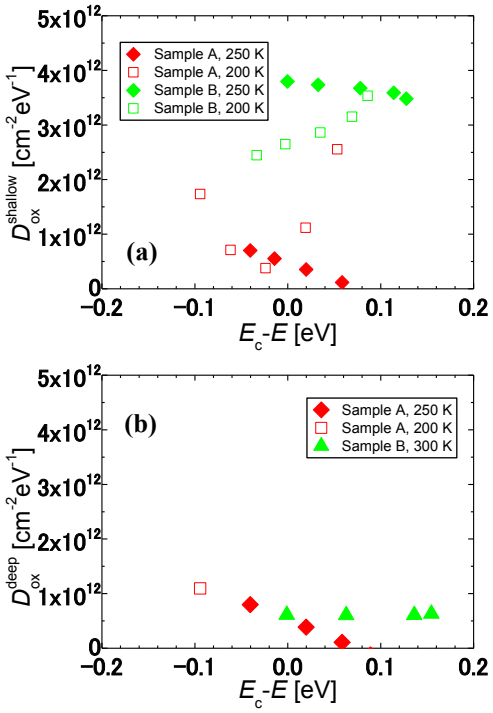

Fig. 5 (a) $D_{\mathrm{ox}}^{\mathrm{shallow}}$ and (b) $D_{\mathrm{ox}}^{\mathrm{deep}}$ of the samples estimated by the measurements at different temperatures.

5. Conclusions

We quantitatively characterized the state density of near-interface oxide traps in SiC MOS capacitors using transient capacitance measurements at various temperatures. There were two groups of oxide traps existing in spatially shallow region and deep region. Our results indicate that $D_{\mathrm{ox}}^{\mathrm{shallow}}$ is an important parameter to characterize SiC MOS quality, in addition to D_{it}.

Acknowledgements

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