Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp510-511

Special Features in Stress Degradation of SiC-MOSFETs Observed in I-V Characteristics

Eiichi Murakami, Kazuhiro Oda, and Tatsuya Takeshita

Kyushu Sangyo University
3-1 Matsukadai 2-Chome, Higashi-ku, Fukuoka-shi, Fukuoka, 813-8503, Japan
Phone: +81-92-673-5639 E-mail: eiichi@ip.kyusan-u.ac.jp

Abstract

SiC-MOSFETs have been remarkably developed in recent years, and the main remaining issue is reliability such as high temperature stability and gate oxide integrity. In this presentation, we report some special features observed in I-V characteristics of commercially available SiC-MOSFETs during high voltage and temperature stress. Interface states around conduction band edge and hole-trapping and near-interfacial electron-trapping are suggested to be the key mechanisms in stress degradation when compared with the conventional Si-MOSFETs. In particular, a continuous I_g increase in MOS structure during stress is found for the first time.

1. Introduction

SiC-MOSFETs have attracted great attention as a key device for future power electronics. Serious mobility problem has been cleared by novel NO-process technique to eliminate interface states drastically. However, reliability issues such as high temperature stability and gate oxide integrity are still important research subjects, in particular for automotive use and from fundamental points of view.

In this presentation, some special features of stress degradation of SiC-MOSFETs are presented when compared with Si-MOSFETs. First, instability in linear I_{ds}-V_{gs} characteristics by positive and negative bias temperature stress (PBTI and NBTI [1][2]) are examined. Second, changes in I_g-V_{gs} and I_{ds}-V_{gs} characteristics by Fowler-Nordheim stress are discussed where a continuous I_g increase phenomena during stress is found for the first time.

2. Experimental

Commercially available 3-terminal SiC-MOSFETs and Si-MOSFETs are measured and heavily stressed (far beyond practical use conditions) by Keysight B2902A source measure unit and 200°C-resistant triaxial cables in high-temperature chamber (ESPEC STH-120). Kelvin connection to source and drain terminal is necessary to eliminate parasitic resistance. In the measurement of I_{ds}-V_{gs} characteristics, we use low V_{ds} voltage (0.05 V) to monitor the impact of interface states and oxide-trapped charge. In FN stress experiments, I_g-V_{gs} characteristics were measured at the same time.

3. Results and Discussion

Degradation in I_{ds}-V_{gs} Characteristics by PBT and NBT Stress

In Fig. 1, change in linear I_{ds}-V_{gs} characteristics is shown during PBT stress. It is mainly positive ΔV_{th}-shift, which suggests electron-trapping in the oxide. Clear recovery phenomena [2] by negative V_{gs} sweep were also confirmed.

In contrast, as shown in Fig. 2, linear I_{ds}-V_{gs} characteristics after NBT stressing are more stretched [1]. Collapse of shoulders in $\log(I_{ds})$-V_{gs} characteristics is remarkable as well as negative ΔV_{th}-shift. This collapse corresponds to gradual rise of I_{ds} around V_{th} in I_{ds}-V_{gs} characteristics.

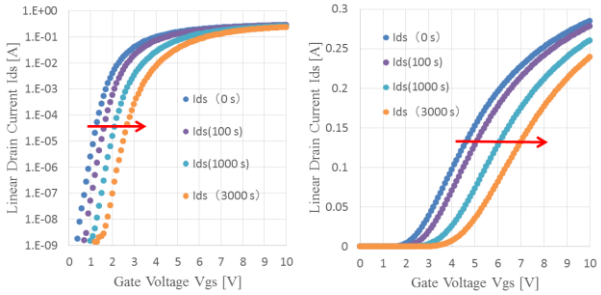

Fig. 1 Linear I_{ds}-V_{gs} characteristics (sweep:0-25V) of SiC-MOSFET during PBT stress (35V, 175℃).

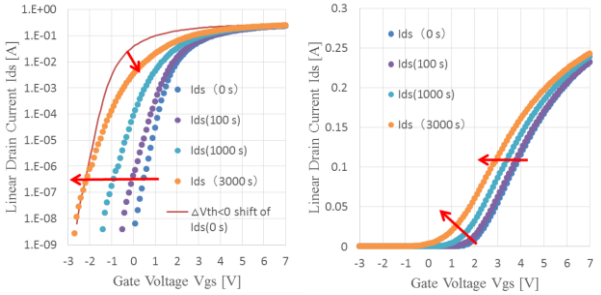

Fig. 2 Linear I_{ds}-V_{gs} characteristics (sweep:-10-25V) of SiC-MOSFET during NBT Stress (-25V, 175℃).

These behaviors can be attributed to the impact of interface states on surface potential $\psi_s(\propto \log(I_{ds}))$ and carrier density Q_n. In Fig. 3, its impact is calculated analytically on the basis of the solution of Poisson equation for MOS capacitor [3].

$$\cdot Qs(\psi s) = Qd + Qn$$
$$= \pm\sqrt{2\varepsilon_{si}kTNa\left[\left(e^{-q\psi s/kT} + \frac{q\psi s}{kT} - 1\right) + \frac{ni^2}{Na^2}\left(e^{q\psi s/kT} - \frac{q\psi s}{kT} - 1\right)\right]}$$
$$\cdot Qit(\psi s) = q\int_{Ev}^{Ei} Dit_D(E)\{(1 - f_D(E,E_F,T)\}dE - q\int_{Ei}^{Ec} Dit_A(E)f_A(E,E_F,T)dE$$
$$\cdot E_F = Ei - q\psi B + q\psi s$$
$$\cdot V_{gs} - V_{FB} = Vox + \psi s = -\frac{Qs(\psi s) + Qit(\psi s)}{c_{ox}} + \psi_s$$

Fig. 3 Analytical calculation of impact of interface states Q_{it} on surface potential ψ_s and surface charge Q_s (=Q_d+Q_n). $\psi_s(V_{gs})$ and $Q_s(V_{gs})$ can be derived from these equations.

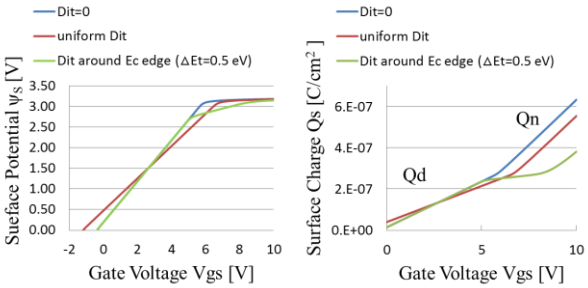

Fig. 4 Calculated results showing the impact of interface states Q_{it} on surface potential $\psi_s(\propto \log(I_{ds}))$ and surface charge $Q_s(=Q_d+Q_n)$.

As shown in Fig. 4, the gradual increase in ψ_s and Q_s was derived when assuming the existence of interface state density D_{it} around conduction-band edge, which can explain the collapse of shoulder in $\log(I_{ds})$-V_{gs} curve and the gradual rise of I_{ds} around V_{th}, respectively.

Degradation in I_{ds}-V_{gs} and I_g-V_{gs} Characteristics by FN Stress

In Fig. 5, I_g-V_{gs} and I_{ds}-V_{gs} characteristics of Si-MOSFETs during FN stressing are shown. Well-known hole-trapping ($\Delta V_{th}<0$, $\Delta I_g>0$) and successive electron-trapping ($\Delta V_{th}>0$, $\Delta I_g<0$) and Q_{it} formation (increase in subthreshold slope) [4] were confirmed from both characteristics.

In contrast, SiC-MOSFETs show totally different behavior. Continuous hole-trapping as well as Q_{it} formation are suggested from I_g-V_{gs} and I_{ds}-V_{gs} characteristics, respectively (Fig. 6). Stress-time dependence of the gate current shown in Fig. 7 clearly shows the remarkable difference in Si and SiC-MOSFETs.

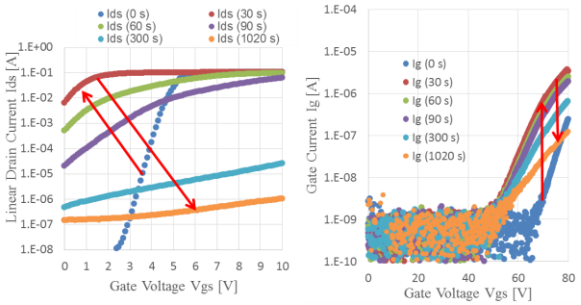

Fig. 5 Linear I_{ds}-V_{gs} and I_g-V_{gs} characteristics (sweep:0-80 V) of Si-MOSFET during FN stress (100V, RT).

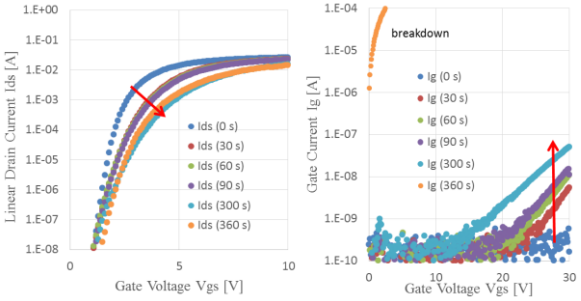

Fig. 6 Linear I_{ds}-V_{gs} and I_g-V_{gs} characteristics (sweep:0-30 V) of SiC-MOSFET during FN stress (50V, 150℃).

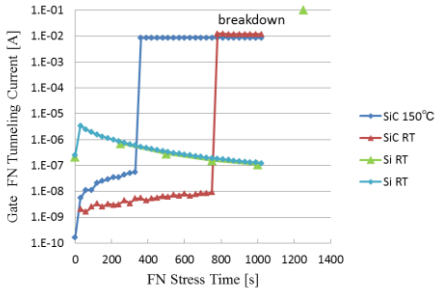

Fig. 7 Stress-time dependence of the gate current in Si and SiC-MOSFETs. Continuous I_g increase was observed in SiC-MOSFETs just before breakdown.

By negative V_{gs} sweep during FN stressing, large negative V_{th} shift suggesting electron detrapping (Fig. 8 (a)) and no remarkable difference in I_g were observed. This easy detrapping nature and little impact on I_g suggested that these negative charges are located near the SiO_2/SiC interface (Fig. 8 (b)). It is shown that interface states have little impact on I_g in Si-MOSFETs with 15 nm thick oxide [5].

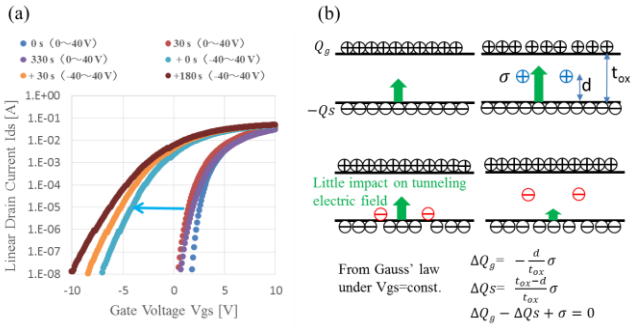

Fig. 8 (a) Negative V_{th} shift by negative V_{gs} sweep meaning electron-detrapping. It should be noted that final $\Delta V_{th}<0$ means trapped holes remain. (b) An illustration of charge trapping in the oxide. Near-interfacial electron can detrap easily and little impact on FN tunneling.

4. Conclusions

We observed some special features in stress degradation of SiC-MOSFETs when compared with Si-MOSFETs. One is I_{ds}-V_{gs} characteristics after NBT and FN stressing, which can be attributed to interface states around E_c. The other is continuous I_g increase by FN stress, which means dominant hole-trapping in the oxide. In addition, near-interfacial electron-trapping (and detrapping) [1, 2] were also confirmed by PBT and FN stress experiments.

Acknowledgements

The authors thank H. Aono, M. Ogasawara, and other members of Renesas Electronics Corporation for financial support and discussions, and S. Miyazaki of PT solutions for technical supports in PC-controlled measurement system.

References

[1] A. J. Lelis, et al., IEEE Trans. Electron Devices **62** (2015) 316.
[2] H. Yano, et al., IEEE Trans. Electron Devices **62** (2015) 324.
[3] Y. Taur, et al., *Fundamentals of Modern VLSI Devices* (2009)150.
[4] E. Y. Wu, et al., *Reliability Wearout Mechanisms in Advanced CMOS Technologies* (2009) 210.
[5] H. Aono, et al., *Proc. Int. Rel. Phys. Symp.* (2006) 71.