Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp518-519

A 150 A SiC VMOSFET with 6 x 6 mm^2 chip size on a 150 mm C-face in-house epitaxial wafer

Yu Saitoh, Hironori Itoh, Keiji Wada, Mitsuhiko Sakai, Taku Horii, Kenji Hiratsuka, So Tanaka, and Yasuki Mikamura

Sumitomo Electric Industries, Ltd.
1-1-3, Shimaya, Konohana-ku, Osaka 554-0024, Japan
Phone: +81-6-6466-5754 E-mail: saitou-yuu@sei.co.jp

Abstract

150 A was successfully generated by a 6 x 6 mm^2 SiC MOSFET chip at *Vds*=2 V and *Vgs*=18 V. A low specific on-resistance V-groove gate structure was utilized with in-house epitaxial growth technology over 150 mm diameter C-face 4H-SiC substrate. Its superior uniformity also realizes high production yield with 1,200 V class breakdown voltage, which gives SiC MOSFET a first and wide path into multi-chip high power module application areas.

1. Introduction

The V-groove trench SiC MOSFET (VMOSFET) with (03-3-8) channel has been proposed as a lower resistivity power device [1-4]. The channel structure is influential on the device performance and is defined by the doping concentration balance between n-type drift layer and implanted p-type regions. The drift layer of VMOSFET is epitaxially grown on C-face 4H-SiC substrate by chemical vapor deposition (CVD). Though epitaxial growth on C-face substrate takes advantage of high conversion ratio of basal plane dislocation into edge type, it has been difficult to ensure uniform carrier concentration over the whole area, especially for 150 mm diameter wafers [5, 6]. In this paper, dealing with n-type epitaxial grown drift layer of VMOSFET fabricated on 150 mm diameter C-face 4H-SiC epitaxial wafer, we investigate effects of carrier concentration uniformity on device properties. We also demonstrate characteristics of the practicable VMOSFET with 6 x 6 mm^2 chip size. Uniformity of the device properties is also promising for high current density power module consisted of multiple chips.

2. Device structure and epitaxial growth

Figure 1 shows the intersectional view of the schematic cell structure of VMOSFET which has buried p^+-regions between the n-type lower and upper drift layers for over 1,000V breakdown voltage.

A hot wall lateral CVD reactor with single wafer susceptor rotating on the center axis was utilized. Epitaxial layers were grown on 4 deg.-off 150 mm n-type 4H-SiC substrate with precursors of SiH_4 and C_3H_8 and H_2 as a carrier gas. The dopant of n-type layer was nitrogen. The lower drift layer on the substrate was followed by ion-implantation for the buried p^+-region. Then, on the upper drift layer regrown epitaxially, the p-well, n^+- and p^+-regions were also fabricated by ion-implantation.

In advance of the device fabrication, epitaxial growth condition was adjusted to be the average carrier concentration of $7x10^{15}$ cm^{-3} for both drift layers. Carrier concentration was measured by capacitance-voltage measurements with a mercury probe on 25 points which were located with 10 mm spacing on orthogonal lines including the wafer center. As the carrier concentration uniformity, the standard deviation from the average, was 15.3 %, we optimized the epitaxial growth condition in order to improve the uniformity.

Figure 2 shows carrier concentration of the drift layer within 150 mm substrate grown by the optimized growth condition. The carrier concentration uniformity is 2.6 % to the average of $6.9x10^{15}$ cm^{-3}. This high quality carrier concentration uniformity is achieved by optimization without losing other properties of the epitaxial layer.

3. Device fabrication and characteristics

Two kinds of (a) conventional and (b) optimized drift layers, of which uniformity is 15.3 % and 2.6 % respectively, were used for device fabrication and device properties such as breakdown voltage and specific on-resistance were compared. Specific on-resistance was measured for test-element-group which was inflated by the influence of unoptimized device dimensions so that it was able to be compared in their relative value not in the absolute one. Fig. 3 shows the relations of device properties to the carrier concentration. The carrier concentration (a) is changed widely in comparison with (b). It is also seen that the deviation of both breakdown voltage and specific on-resistance of (b) increase with distance from the average rather than (a). However, this deviation is larger than the change of drift resistance expected by the difference of the carrier concentration. It is estimated that the position of the interface between the p-well and the n-type drift layer is changed by the carrier concentration variation within the wafer and has an influence on channel resistance. *Id*=150 A at *Vds*=2 V, *Vgs*=18 V was also obtained by the practicable 6 x 6 mm^2 chip (Fig.4).

4. Conclusions

The optimized epitaxial layer can improve the carrier concentration uniformity which has influence on the specific on-resistance of VMOSFET through the drift resistance and channel resistance. The practicable large size VMOSFET demonstrate over *Id*=100 A at *Vds*=2 V. Uniformity in such device properties gives advantage for high current density power module application.

References

[1] T. Masuda *et al*., Material Science Forum, vols. 778-789, pp. 907-910 (2014).

[2] Y. Saitoh *et al*., Material Science Forum, vols. 778-780, pp. 921-934 (2014).

[3] K. Wada *et al*., in Proceedings of 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD), pp.225-228 (2014).

[4] K. Uchida *et al*., 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), pp. 85-88.

[5] H. Tsuchida *et al*., Material Science Forum, vols. 572-529, pp. 231-234 (2006).

[6] A. Miyasaki *et al*., Material Science Forum, vols. 778-780, pp. 193-196 (2014).

.

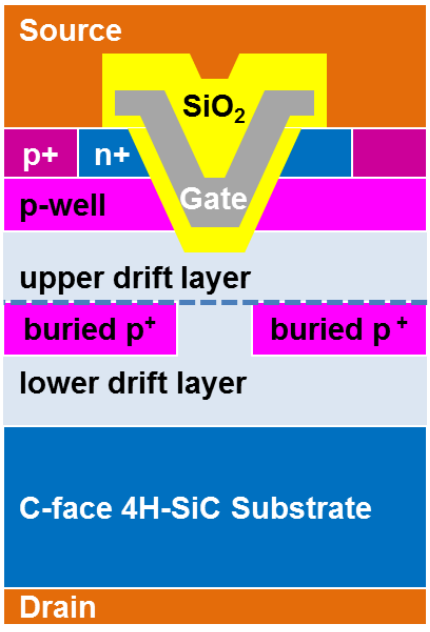

Fig. 1. Schematic view of intersection cell structure of VMOSFET. The dashed line between upper and lower drift layers is epitaxial regrowth interface.

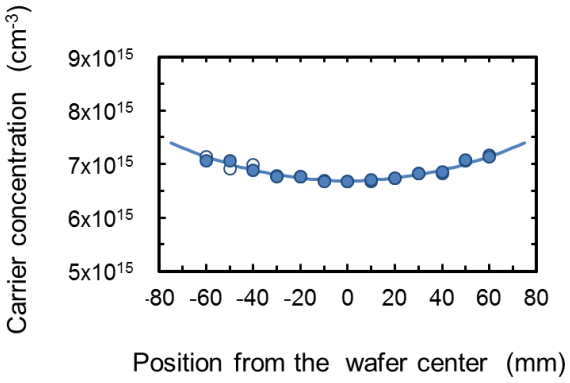

Fig. 2. Carrier concentration of the drift layer within 150 mm epitaxial wafer grown by optimized growth condition. The carrier concentration uniformity is 2.6 % for the average carrier concentration of 6.9×10^{15} cm^{-3}.

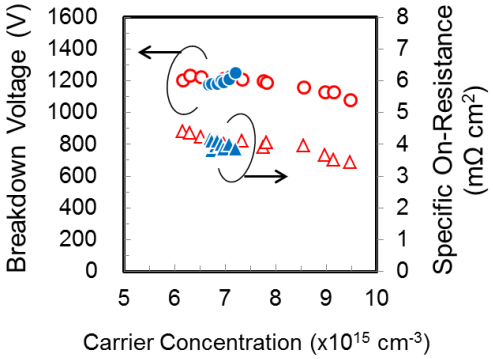

Fig. 3. Breakdown voltage (circle) and specific on-resistance (triangle) to carrier concentration. Opened and filled symbols are for epitaxial wafers of (a) and (b), respectively.

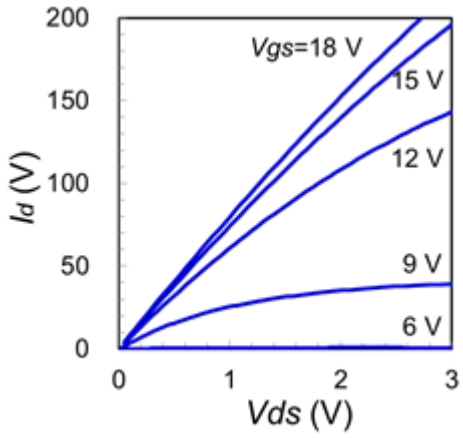

Fig. 4. *Id-Vds* curve at *Vgs*= 6, 9, 12, 15 and 18 V of VMOSFET with 6 x 6 mm^2 chip size.