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The Resistance Effect on Turn-On Speed of Resistor Assisted Trigger SCR Stacking Structure

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Abstract

The resistance effect on turn-on speed in resistor assisted trigger stacking SCR structure has been investigated for on-chip electrostatic discharge (ESD) protection in a 0.11 μm high-voltage (HV) 32V CMOS process. We have successfully eliminated the double snapback characteristic by using an embedded substrate resistance as trigger resistor in resistor assisted trigger SCR stacking structure. A holding voltage is achieved as higher as about 21 V, no additional trigger voltage increase.

1. Introduction

Silicon-controlled rectifier (SCR) is an attractive elements for ESD protection application because it can sustain the highest ESD stress compared with other ESD devices **[1]**. When SCR is triggered, the extremely low holding voltage would allow SCR change to a high-conductive state to release the ESD charge. Nevertheless, such a low holding voltage (V_h) could induce a latch-up issue in high voltage (HV) operation, if the holding voltage of SCR is smaller than the supply voltage (V_{cc}). Once latch-up occurs, HV CMOS ICs are inevitable to be damaged due to high power generated by latch-up. In 2013, a ring-resistance-triggered (RRT) technique was proposed to obtain a high holding voltage and only a tiny trigger voltage (V_{t1}) increase **[2]**. However, the resistance effect of the ring resistor and the detail trigger mechanism are not revealed. In order to clarify the resistance effect in resistor assisted trigger SCR stacking structure, we adopt the polysilicon resistor (R_{poly}) and a p-substrate resistor ($R_{p\text{-}sub}$) as triggered elements.

2. Device Design of Unit SCR Cell

The structure of sample is a segmented emitter topology lateral SCR (SLSCR) that is based on a symmetric n-LDMOS structure. Figure 1 shows the schematic of SLSCR, which has been demonstrated the V_h increasing with reducing minority carrier injection from emitter to base due to decreasing emitter area of the two parasitic BJTs existed in SCR structure [3-4]. However, scale down emitter area would lead a poor conduction ability due to serious current crowding, which resulted in an obviously decrease of second breakdown current (I_{t2}). In order to attain high V_h and FOM simultaneously, the optimized ratio of S/T is 1, listed in Table I.

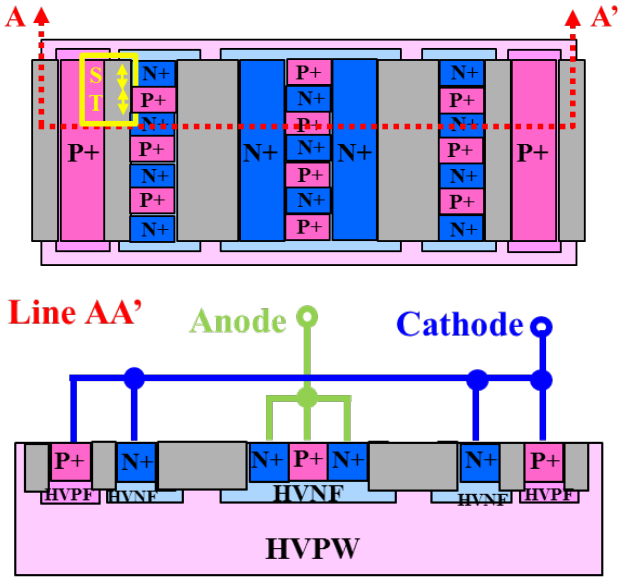

Fig. 1 The schematic of SLSCR.

Table I Comparison of FOM for different S/T ratio

S:T	V_{t1} (V)	V_h (V)	I_{t2} (A)	FOM $V_h \times I_{t2}$ (W)
1:0	40.48	8.76	4.00	35.04
3:2	38.45	10.34 (18%↑)	3.61 (10%↓)	37.32
1:1	38.55	10.62 (21%↑)	3.37 (15%↓)	35.78
2:3	38.50	11.64 (33%↑)	2.17 (46%↓)	25.25

3 TLP Measurement and Discussion

For achieving high holding voltage SCR without increasing the trigger voltage, the resistor assisted triggered SCR stacking structure technique is employed **[2]**. The equivalent circuit configuration is expressed as shown in Fig. 2(a). It includes two SCR and one resistor in this equivalent circuit. As the first stage SCR_1 is turned on, the ESD current flows through the resistor R_2, which results in an electric potential redistribution across the anode and cathode. Once the voltage drop of R_2 is higher than the trigger voltage of SCR_2, the SCR_2 is turned on. For rapidly turning on SCR_2, a modified SLSCR (here called SMLSCR) structure was used instead of SCR_2. The schematic structure of SMLSCR is shown in Fig. 3(a). The TLP

I-V characteristic of SLSCR and SMLSCR are depicted in Fig. 3(b). Both of SCR have similar holding voltage of 10.5V, but the trigger voltage of SLSCR and SMLSCR are 38.5V and 25V, respectively. An interesting phenomenon of double snapback is observed as shown in Fig. 4. In the cases of R_2= R_{poly}= 40, 60, and 80Ω, all of them have a second trigger point at about 35V. However, once trigger resistor R_2 is replace by an embedded substrate resistor $R_{p\text{-}sub}$, the double snapback behavior is eliminated. Generally, the doping concentration of p-Substrate is $\leqq 10^{16}$ #/cm^3. Such low doping concentration in p-substrate can easily lead a very high resistance $R_{p\text{-}sub}$ of ~ kΩ in a layout structure without iso-HVNW layer drawing between two stacks SCRs (SCR_1 and SCR_2). After SCR_1 is turn-on, the equivalent circuit component can be considered as one voltage source V_h and one resistor R_{SCR1}. If R_2= $R_{p\text{-}sub}$>> R_{SCR1}, the voltage drop of SCR_2 is equal to voltage drop of anode to cathode (V_{ac}) deduct from the holding voltage of SCR_1 ($V_{h,\ SCR1}$) (ie. V_2= V_{ac} –$V_{h,\ SCR1}$= $V_{t1,\ SCR1}$ –$V_{h,\ SCR1}$). This can be easily realized by divided voltage law in the circuity. Consequently, SCR_2 can be triggered rapidly after SCR_1 is turned on.

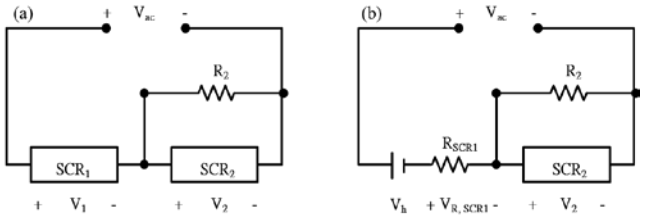

Fig. 2 The equivalent circuit configuration of resistor assisted trigger SCR stacking structure, (a) before SCR_1 turn on and (b) after SCR_1 turn on.

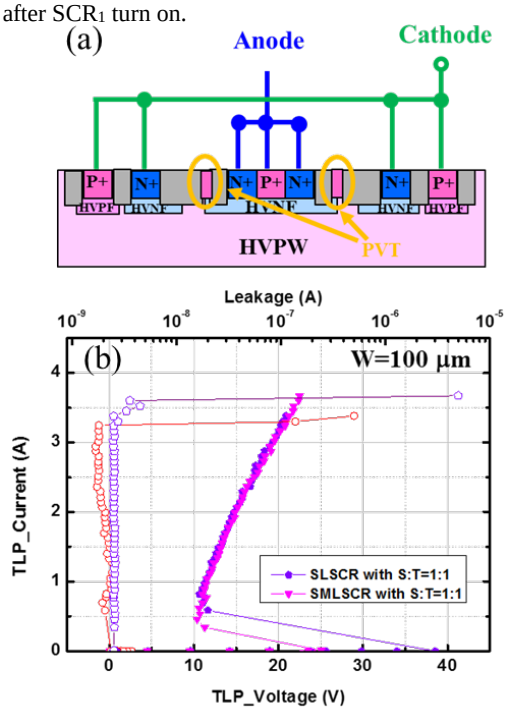

Fig. 3 (a) The schematic structure of SMLSCR (b) The TLP I-V characteristic of SLSCR and SMLSCR

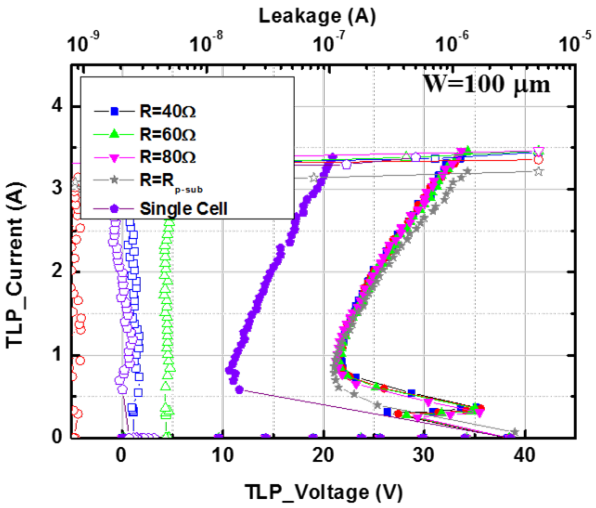

Fig. 4 The TLP I-V curve of resistor assisted trigger SCR stacking structure with different R_2.

4 Conclusions

Removing the iso-HVNW of the resistor assisted triggered SCR stacking structure can generate a very large parasitic substrate resistance of R_2 in 0.11 mm HV 32V CMOS process. Once SCR_1 is triggered, a voltage drop of about V_{ac}- $V_{h,\ SCR1}$ will be immediately across on SCR_2 after electric potential redistribution. Therefore, a high holding voltage without extra increased of V_{t1} and double snapback fast turn-on speed SCRs stacking structure is successfully fabricated.

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References

[1] V. A. Vashchenko et al., *IEEE Trans. Device Mater. Rel., Vol. 4, No. 2, (2004) 273-280*

[2] F. Ma et al., *IEEE EDL Vol. 34, No. 9, (2013) 1178-1180.*

[3] Z. Liu et al., *IEEE EDL Vol. 29, No. 7, (2008) 753-755.*

[4] C.-Y. Hung et al., *EL Vol. 50, No. 3, (2014) 200-202.*