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Impact of 3D stacking silicon on diamond substrate for the ESD protection device

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Abstract

In this paper, ESD protection capability of the protection devices fabricated on Silicon on Diamond (SOD) structure and the conventional Si substrate is compared. The results showed that ESD protection capability of the SOD substrate is 2.8 times higher than that of SOI substrate. In additions, we propose the 3D stacking structure suitable for power supply on chip (power-SoC) and the best location for implementation of the ESD protection device based on device simulations.

1. Introduction

Recently, power supply on chip (power-SoC) have been attracted attentions of many researchers because it can realize ultimate minimization of the power supply[1]. One of the effective ways to shrink the size of the power supply is to reduce the volume of the passive components such as inductors and capacitors. Increasing the switching frequency of power supply is one of the most promising approaches to do this. SOI structure is attracting attention as devices operating at high frequencies. However, the thermal conductivity of the oxide film is small and it faces the problem of decreasing ESD protection capability. An SOD (Silicon on Diamond)[2] structure is promising to overcome the problem of ESD capability because it can effectively exhausting heat. Recently, 3D stacked power-SoC has been attracted it can realize much higher density integration and heterogeneous integration such as Si LSI and GaN power devices. In 3D system, ESD protection is also one of the key issues. In such schemes, this paper proposes the ESD protection devices suitable for SOD substrate. In addition, this paper also describes the 3D stacking structure suitable for power SoC and the best location for implementation of ESD protection devices.

2. Device structure and the element failure criterion

ESD protection capability is evaluated by HBM model [3] through device simulation [4]. The circuit diagram for HBM test is shown in Fig. 1. (DUT: Device Under Test) The material constants used in this simulation are

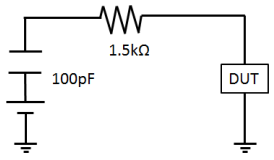


Fig. 1 The simulated circuit configuration.

Table.1 Material constants used in simulations.

Parameter	Si	SiO_2	Diamond	Air
Specific heat [J/kg/K]	700	780	520	1000
Density [kg/m^3]	2330	2200	3500	1.2
Thermal conductivity [W/m/K]	145	1.4	20	0.026

listed in Table 1. The thermal conductivity of diamond film is assumed to 20 $Wm^{-1}K^{-1}$, which is the thermal conductivity of nano-crystalline diamond formed by plasma CVD[5]. In this paper, we assume destruction of an ESD protection device is caused by its self-heating [3]. First, we measured the power density experimentally when the pn junction diode breaks at reverse bias mode. The power is determined by I-V characteristics. Power density at the time of device destruction was 5.58×10^{-3} [μm^3 / W]. Next, we estimate the temperature of the pn diode using the device simulation at the input power density of 5.58×10^{-3} [μm^3 / W]. The temperature is 551 [K] when the input power density of 5.58×10^{-3} [μm^3 / W] and we define 551 [K] as a temperature at which the device breaks.

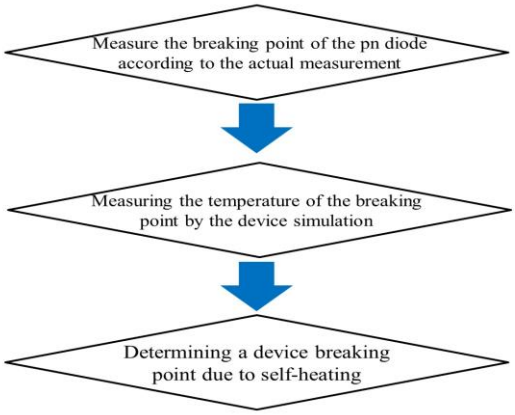
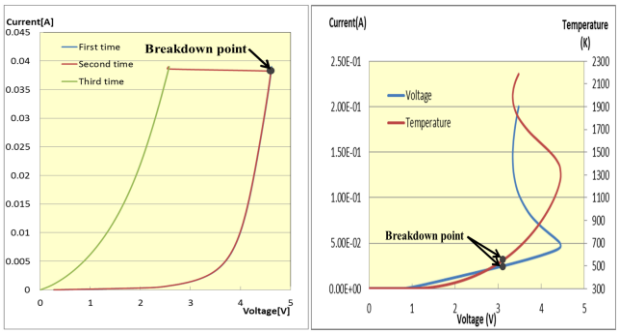


Fig. 2 Determination of temperature at device destruction.

3. Results and discussion

The HBM capability is compared in Table 2. That of the protection devices formed on SOD substrate is always larger than those formed on the conventional SOI substrate. HBM capability of the conventional MOSFET formed on SOD is largest and 719 V. HBM capability of the MOSFET fabricated on SOD substrate is 2.8 times higher than that on the conventional SOI substrate because temperature of the active layer of the SOI MOSFET is higher than that fabricated on SOD substrate.



(a) measured (b) simulated

Fig. 3 I-V characteristics of the diode.

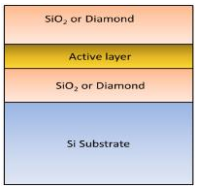
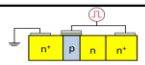
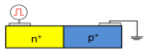
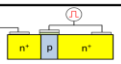
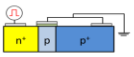
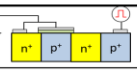


Fig. 4 Simulated substrate structure.

Table 2 Comparisons of HBM capability.

	The active layer structure	HBM voltage	
		SOI substrate	SOD substrate
#1		128	211
#2		281	587
#3		260	719
#4		147	277
#5		234	527

The simulated 3D stacking structure is shown in Fig. 5. The ESD protection device is fabricated on Si_1 or Si_2. Comparisons of HBM capability of various 3D stacking structures are shown in Fig. 6. The active layer means the location of the ESD protection device fabrication. In these simulations, the MOSFET is used as the ESD protection device and the structure is optimized to realize higher ESD capability. Insulator_1, Insulator_2, and Insulator_3 are SiO2 or diamond.

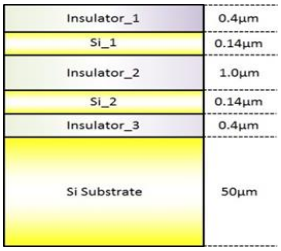
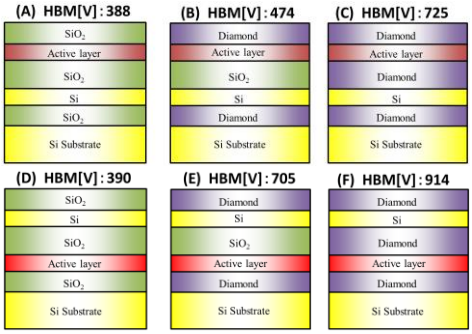


Fig 5 Simulated 3D stacking structure.

HBM capability is the highest when the diamond films are used as all insulator films. In this case, HBM capability is 914 V. In addition, the ESD protection capability is higher in the case of diamond film used as the insulator film when the device was fabricated on lower semiconductor layer because the heat capacity is larger owing to thick Si substrate below the diamond. Figure 7 shows the transient temperature response when the ESD protection device works. Insulator_1 and Insulator_3 are diamond films. The HBM capability of the structure (F), which uses diamond film used as Insulator_2, is the highest, however slightly rises temperature of Si_2. Temperature rise of structure (E), which uses SiO2 as Insulator_2, is suppressed, but HBM capability of that is about 200 V lower.



Figs. 6 Comparison of HBM capability for SOI and SOD.

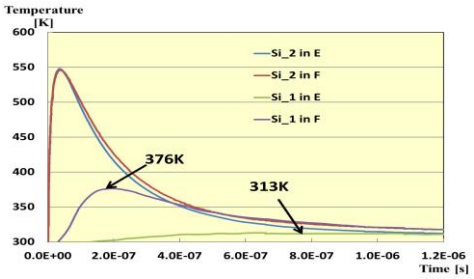


Fig. 7 Transient temperature response.

3. Conclusions

We evaluate the ESD protection capability of the ESD protection devices based on device simulations. The ESD protection capability of device fabricated on SOD is larger. The MOSFET is the suitable for ESD protection device fabricated on SOD substrate. When we implement the ESD protection device on 3D stacking power-SoC structure having diamond films as insulator films, we prefer to implement the protection device on lower semiconductor layer.

References

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