

Improved electrical properties of 4H-SiC MOS devices with high temperature thermal oxidation

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Abstract

Capacitance-voltage characteristics of SiO₂/4H-SiC (0001) MOS capacitors fabricated by the different thermal oxidation conditions are compared. The dependence of oxidation temperature on device characteristics (such as V_{FB}) is analyzed. At higher oxidation temperature the device reliability of SiC MOS are improved. Such behavior can be attributed to the reduction of the interface traps.

1. Introduction

Silicon Carbide (SiC) has been commercially accepted as an alternative semiconductor for power MOS devices due to attractive properties, such as high breakdown-field and high thermal conductivity, which are suitable for high-voltage power and high energy-efficiency electronic devices^[1,2]. In addition, SiO₂ films can be grown on SiC substrates by conventional thermal oxidation, which is one of the unique advantageous of SiC over other wide-gap semiconductors in device fabrication. However, thermal oxidation of SiC has been believed to induce a large number of interface defects at the SiO₂/SiC and near-interface traps considerably. The interface defects not only reduce the channel mobility of SiC-MOS field-effect-transistors (FETs) transistors but also decrease the performance reliability. For the reduction of those interface defects on 4H-SiC, various passivation techniques including annealing in NO_x treatment have been reported to work effectively to reduce the interface traps in (0001) face 4H-SiC^[3,4], but the effective mobility is just only several 10 cm²/V s. For (000-1) face 4H-SiC, pyrogenic gate oxidation followed by H₂ POA has been reported to suppress the formation of those defects, and the peak value of μ_{FE} for SiC MOSFETs is up to 111 cm²/V s, which is much higher than that of SiC MOSFETs fabricated on Si (0001) faces^[5]. However, Hatakeyama also reported that dislocations such as threading screw dislocations (TSDs), threading edge dislocations (TEDs) and basal plane dislocations (BPDs), are not correlated with the reliability of the MOSFETs on the C-face of 4H-SiC^[6]. F. Devynck and V. V. Afanas have reported that the residuced carbon are the most possible origin of the interface defects on 4H-SiC^[7,8]. For further reduction of the interface traps, we found the optimizing oxidation conditions is better for elimination of carbon-related byproducts.

In this study, we investigate the effects of the oxidation temperature on the distribution of carbon and oxygen vacancy in the SiO₂/4H-SiC interface respectively. The defects generation mechanism and the degradation of SiO₂/SiC interface in the SiO₂/SiC system are investigated.

2. Experiments and results

We fabricated SiO₂/SiC capacitors on 4H-SiC (0001) substrate with an n-type epitaxy layer ($N_D = 1 \times 10^{16}$ cm⁻³). After RCA cleaning, a 4H-SiC (0001) wafer with n-type ($\sim 1 \times 10^{16}$ cm⁻³) epitaxial layer was cleaned by dipping in hydrofluoric acid (HF) to remove sacrificial oxide layer. The samples were then immediately loaded into an oxidation furnace and oxidized in dry O₂ ambient from 1200°C to 1350°C for various durations. This dry oxidation process was kept at 880 mbar pressure with an oxygen flow rate of 2 L/min. Since it has been reported that several electrical degradations are caused by thick thermal oxides^[6], post-oxidation treatments including N₂ annealing at the oxidation temperatures for 30 min, and O₂ annealing at 1000°C for 1 min were performed to reduce the interface trap density and the electron traps in SiO₂ dielectrics during high temperature oxidation. Note that all oxidation processes in this experiment were conducted in the mass production furnace with a 1400°C maximum temperature range. Finally, 200 nm Al were sputtered as the back and gate electrodes for the MOS capacitors.

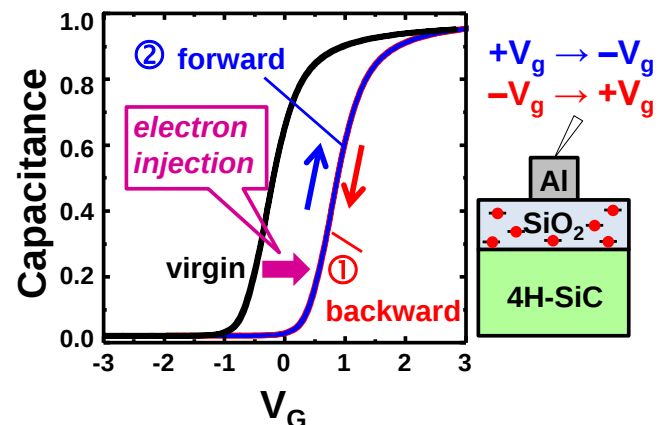


Fig. 1 Measurement sequence of C-V cures.

The bidirectional capacitance-voltage (C-V) characteristics of the fabricated MOS capacitor measured with Agilent

1500B, and the ideal flat band voltage calculated by theory quotation is shown in Fig 1. The C-V curves are described as ‘virgin’ C-V curves. After the electron injection, we carry out ‘backward’ and ‘forward’ C-V sweep in the same MOS capacitor.

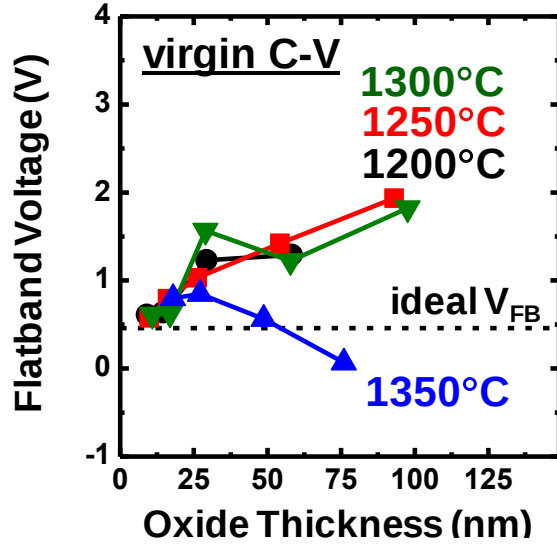


Fig. 2 Flat band voltages before electron injection.

The results indicate that the oxide thickness varies at different oxidation temperature from 1200 to 1350°C. The oxidation temperature dependence parameters such as V_{FB} (‘virgin’ C-V curves flat band shifted from the ideal flat band) and the oxide thickness are shown in Fig. 2. The ideal V_{FB} (dot line) are also calculated (0.46eV). It is clearly observed that V_{FB} shows positive shifts and increased with oxide thickness under thermal oxidation of temperatures below 1300°C, which indicated that the numbers of negative fixed charges generated after thermal oxidation of the temperatures are compared (V_{FB} are increasing in the same trend). However, the V_{FB} increase varied from 0 to 25nm and then decrease to a negative V_{FB} shifts, which are slight governed by ‘positive charges’, under the oxidation temperature in 1350°C.

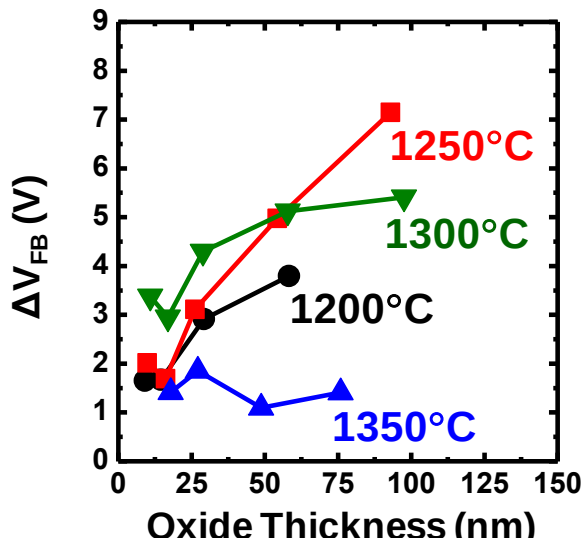


Fig. 3 Flat band voltages after electron injection.

After stressing by positive gate voltage for 1 min, V_{FB} shift due to electron injection at room temperature (shown as Fig. 3). A shift of V_{FB} was observed due to electron traps. The shift of V_{FB} increase with oxide thickness for the three samples (1200, 1250 and 1300°C), and the samples are compared during the different oxidation temperatures. The MOS device (oxidation temperature for 1350°C) remained stability under the stress. It was found that oxidation temperature have more effective on the device reliability. The V_{FB} shift varied almost 1 V after the gate stress. This shift is so small compared to the typically reported results (oxidation temperature at 1200°C and 1300°C). It is also showed that the V_{FB} shift is much smaller under the lower oxidation temperature. It is assumed that there is may be a balance between the competitive reactions: SiO_2 formation and CO_x desorption.

3. Conclusions

A higher oxidation temperature is benefit to get smaller V_{FB} shift, and these experimental results also show that the optimization temperature is better for improving electrical properties of 4H-SiC MOS devices.

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