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Removal of Near-Interface Oxide Traps at SiO_2/SiC Interface by Post-Oxidation Annealing in Reducing Ambient

Hiroyuki Kajifusa, Hirohisa Hirai, Yuki Fujino, and Koji Kita
Department of Materials Engineering, The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo, 113-8656, Japan
Phone: +81-3-5841-7164 E-mail: h.kajifusa@scio.t.u-tokyo.ac.jp

Abstract

The density of near-interface oxide traps, observed as fixed charges and hysteresis of C-V curves, at 4H-SiC MOS interface with 1250°C-grown thermal oxide was dramatically reduced by 1150°C annealing in diluted H_2 ambient, while interface state density was not affected significantly by the annealing.

1. Introduction

Thermal oxidation of SiC is often suffered from insufficient SiO_2/SiC interface quality with high density of interface defect states and near-interface traps.

There are two approaches to reduce the interface defects: suppression of defect generation by the control of oxidation conditions, and removal of defects by post-oxidation-annealing (POA). As for the former approach, it has been pointed out that the growth in thinner film region is advantageous for the out-diffusion of carbon-related byproducts because of the interface-reaction-limited growth [1]. As for the latter one, POA in various ambient such as Ar and H_2 [2,3] have been reported. In this study we investigated the impacts of both the oxide thickness and the POA on SiC MOS interface quality systematically.

2. Experiments

4H-SiC (0001), Si face, wafers with ~1×10^{16} cm^{-3} doped n-type epitaxial layers were cleaned in diluted HF, followed by the oxidation at 1250°C in 1-atm dry O_2 with the ramp-heating furnace as we previously reported [1,4]. The films with different thicknesses from ~7 to 50 nm were prepared by changing the oxidation time. An additional annealing at 1150°C was conducted in 1%-H_2 + He ambient.

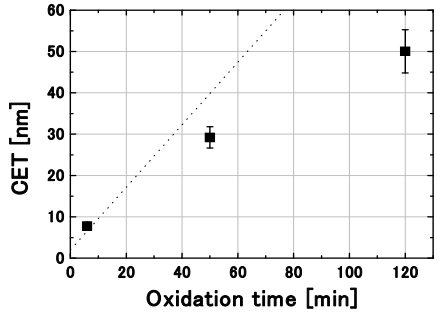


Fig. 1 Relationship between oxidation time and thermal oxide thickness grown at 1250°C in 1-atm-O_2. The vertical axis is the capacitance equivalent oxide thickness (CET). Dotted line is corresponding to the interface-reaction-limitted growth case estimated from [1].

Finally, Au gate electrode was evaporated on top to fabricate MOS capacitors.

3. Results and Discussions

The oxidation rate was found to reduce significantly by increasing the film thickness, as shown in **Fig. 1**. This result indicates that the film growth in ~50 nm-thick region does not proceed in interface-reaction-limited manner for the dry oxidation at 1250°C in 1-atm-O_2, while it has been already reported that the ~15 nm-thick film is thin enough for the interface-reaction limited growth [1]. In "modified Deal-Grove model" of SiC oxidation [5], two kinds of diffusion steps are involved: CO out-diffusion and O_2 in-diffusion. If the former limits the growth rate, the

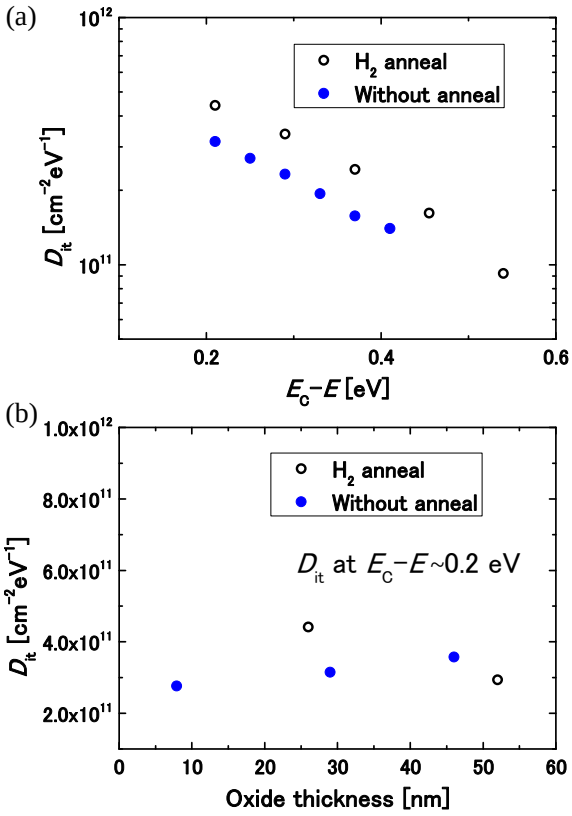
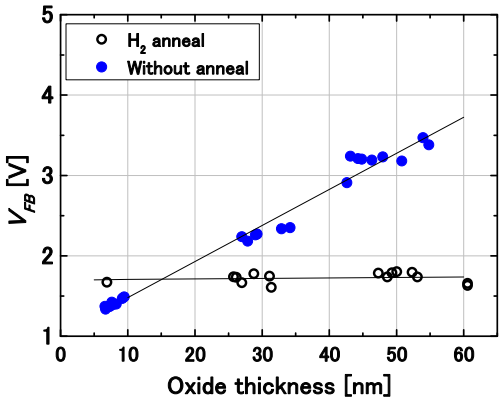


Fig. 2 (a) D_{it} of the MOS capacitors (CET~30nm) with or without 1%-H_2 annealing, as a function of energy level below the conduction band of SiC. D_{it} was measured by conductance method at room temperature. (b) Oxide thickness dependence of D_{it} at E_C-E~0.2eV for the capacitors with or without 1%-H_2 annealing.

(a)



(b)

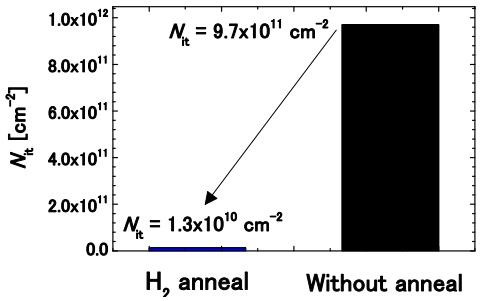


Fig. 3 (a) Oxide thickness dependence of V_{fb} for the MOS capacitors with or without 1%-H_2 annealing. (b) Estimated N_{it} from the slope. N_{it} is significantly suppressed by 1%-H_2 annealing.

interface quality should depend on the film thickness, however, this is not the case if the latter limits the rate [6].

The interface state density (D_{it}) of the samples with various thickness was investigated by conductance method. D_{it} of samples with CET ~30 nm is shown in **Fig. 2(a)**. D_{it} ~10^{11} $cm^{-2}eV^{-1}$ was observed for a wide range of energy, without any introduction of passivating elements. The obtained D_{it} at E_C–E ~0.2 eV is plotted in **Fig. 2(b)** as a function of oxide thickness. D_{it} does not change significantly even when increasing the film thickness up to 50 nm. Thus D_{it} is not significantly affected by the change of growth mode. The discrepancy with a previous report on the thickness-dependent D_{it} [7] will be attibuted to the difference of oxidation conditions.

It is also noteworthy that 1%-H_2 annealing does not have a large impact on D_{it}, as shown in **Fig. 2(b)**. On the other hand, we found that oxide trap density was significantly affected by POA. The thickness dependence of flat-band voltage (V_{FB}) is shown in **Fig. 3(a)**. From the slope we can estimate the interface trap density (N_{it}) by assuming the fixed charges are locating only at the interface, as shown in **Fig. 3(b)**. The N_{it} of 1%-H_2 annealed samples was estimated to be ~10^{11} cm^{-2}, whereas that of non-annealed one was in the order of ~10^{12} cm^{-2}. The hysteresis of C-V curve also well suppressed by 1%-H_2 annealing, as shown in **Fig. 4**. Taking account of our voltage sweeping rate, the reduction of hysteresis width is attributed to the decrease of near-interface oxide traps with a long time constant ~10 s.

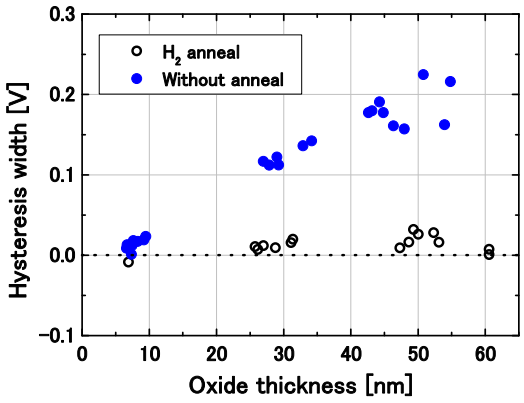


Fig. 4 Oxide thickness dependence of hysteresis width of C-V curves defined at $V_G = V_{FB}$ for the MOS capacitors with and without 1%-H_2 annealing. Positive values indicate clockwise hysteresis and negative values indicate counter-clockwise.

These results clearly show that near-interface oxide defect density is efficiently suppressed by high-temperature annealing in reducing ambient, in contrast to that D_{it} is not so sensitive to the annealing. The reported improvement of inversion channel mobility by H_2 annealing [2] is also attributable to the reduction of near-interface oxide traps. The mechanism of oxide defect removal is not clear at present, but we speculate such annihilation would correlate with the self-decomposition of SiO_2 occurs at SiO_2/SiC interface at >1000°C in UHV [8].

4. Conclusions

4H-SiC (0001) MOS interface quality did not change significantly by increasing the oxide thickness up to 50 nm in our oxidation conditions, but was dramatically improved by a high-temperature annealing in reducing ambient. Especially, the density of near-interface oxide traps, observed as fixed charges and hysteresis in C-V curves was dramatically reduced by the annealing in 1%-H_2 ambient at 1150°C.

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