Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp502-503

Investigation of 4H-SiC IGBT Turn-off Performance for Achieving Low Power Loss

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Abstract

The dynamic operation of a 4H-SiC IGBT turn-off performance is investigated using reported measurements of the interface defect density and device simulation. During the off-state of a repetitive pulse switching, trapped carriers influence the channel potential towards the collector side that creates a path for current flow. The current is observed as an additional tail current that contributes to power dissipation The capture cross-section parameter used in the simulation depicts the probability of traps capturing carriers. Lower parameter value entails longer time for carrier trap/detrap process, and vice-versa. Future scaled SiC-based devices need to achieve an excellent SiC/SiO$_2$ interface to achieve low off-state current and thereby, low power loss.

1. Introduction

The mainstream use of Si in electronic circuits is mainly attributed to the excellent quality of Si/SiO$_2$ interface. Recent high-power switching applications, however, require functions that are beyond the physical characteristics of Si. Therefore, the industry is actively identifying alternative materials. SiC is one candidate because of its wide bandgap, high thermal conductivity and high thermal stability. To fully utilize SiC, one challenging task is to achieve an excellent 4H-SiC/SiO$_2$ interface [1].

Measurements of the defect density of the 4H-SiC/SiO$_2$ interface [2] shows a density magnitude $D_{\rm it}$ of ~10^{13}cm^{-2} eV^{-1} and is characterized by distinct, acceptor-type deep and shallow traps as schematically illustrated in Fig. 1a. The resulting $I_{\rm c}$-$V_{\rm c}$ simulated with the measured trap density is shown in Fig.1b [3]. The switching characteristics at high-frequency has also been reported [4]. While different investigations are reported for the impact of defects, the effect on the device turn-off performance characteristics is not addressed. In this work, we report the impact of interface defects on the turn-off performance characteristics of a 4H-SiC IGBT using the reported measurements of the interface defect density and consistent device simulation.

2. Device Simulation

The investigated IGBT cross section is shown in Fig. 2. Device simulation involves solving the Poisson equation, the carrier continuity equations and the current density equations consistently. The defects are modeled as Gaussian and exponential distributions with parameters extracted from the measurements. The effects of the capture cross section for each distinct trap are included in the transient modeling equations as

$$\frac{d}{dt}(p_{TA}) = \int_{E_v}^{E_C} g_{TA}(E)\cdot\left[\nu_n\cdot SIGTAE\cdot\left(n\cdot(1-f_{t,TA}(E)) - f_{t,TA}(E)\cdot n_i\exp\left[\frac{E-E_i}{kT}\right]\right)\right.$$
$$\left. -\nu_p\cdot SIGTAH\left(p\cdot f_{t,TA}(E)-(1-f_{t,TA}(E))\cdot n_i\exp\left[\frac{E_i-E}{kT}\right]\right)\right]dE$$

where p is the charge contribution, g is the distribution function and f is the probability of occupation of a trap level at energy E. The focus of this work is given on the influence of capture-cross section parameters as shown in Table I.

2.5KHz switching frequency is applied to the gate with $V_{\rm g}$=34V and $V_{\rm c}$ = 15V to obtain a strong inversion condition and current flow.

3. Results and Discussion

Fig. 3 shows the effect of capture cross-section parameters on the decay current during on-state. The conditions are summarized in Table II. The parameters depict the probability of the trap capturing a mobile carrier. A higher cross section gives a higher probability of trapping thereby decreases the current. Condition A has a smallest cross section which means that it takes time until trap states are occupied completely so the degradation also takes time. Condition B has the deep traps completely occupied, and condition C means that shallow trap is occupied completely.

Fig. 4a and 4b show the log plot of collector current taken with a longer off-state gate voltage. The tail current without any defect is purely displacement current. When defects are present, the magnitude of the off-state current is increased. The detrapping of carriers is also governed by the cross section parameters. Condition A has smaller values meaning that carriers take time to be detrapped. In B, the deep trap is high and easily filled but detrapping process is slow. The probability of recombination current due to recombining carriers from the valence and conductions bands is also high because the deep trap is in the mid-bandgap. C, having a big cross-section for the shallow trap, means that carriers can be detrapped easily because lesser energy is necessary.

The presence of off-state currents contribute to the overall device power dissipation. The carriers that are being trapped during the on-state are the ones contributing to the increase of the tail currents. During turn-off, the trapped carriers influence the potential distribution at the collector side of the channel in order to create a path of current flow. The distributions extracted just below the device channel in Fig. 5a are shown in Fig. 5b. Condition B having the greatest electric field contains the most carriers as can be seen in Fig. 4b.

Fig. 6a and b show the currents and the corresponding power dissipated calculated as

$$\Delta P = (I_{\text{with defect}} - I_{\text{without defect}}) * V_c$$

The greatest power dissipated is when the defects are present and capture cross-sections parameters are small. Therefore, power SiC devices should aim for lower defect magnitude and correct characterization of capture cross-section.

3. Conclusions

Interface defects contribute off-state current during a turn-off in a switching condition. The off-state current is observed as an addition to the tail current which induces more power dissipation. For SiC-based devices, an excellent quality of the SiC/SiO_2 interface with smaller defect density magnitude becomes necessary to reduce power consumption.

References

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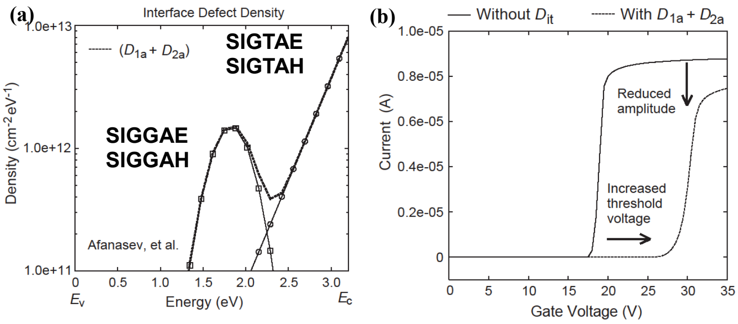

Fig. 1 (a) Measured interface defect densities. (b) DC degradation due to defects: increased threshold voltage and reduced amplitude.

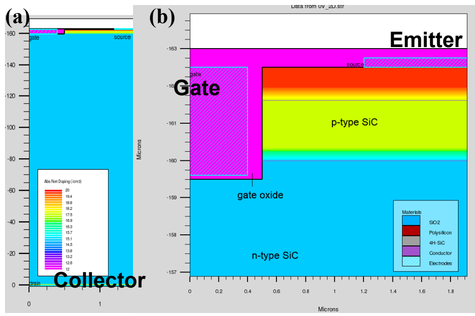

Fig. 2. Channel of the 4H-SiC IGBT structure used in the simulation. (a) Full structure. (b) Channel region

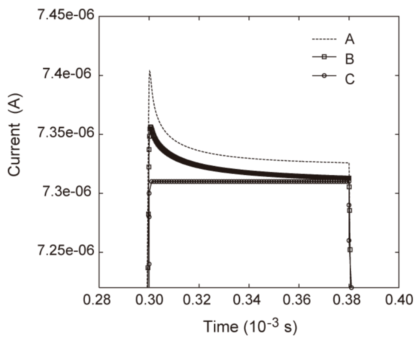

Fig. 3. Effect of capture cross-section parameters on the collector current during on-state.

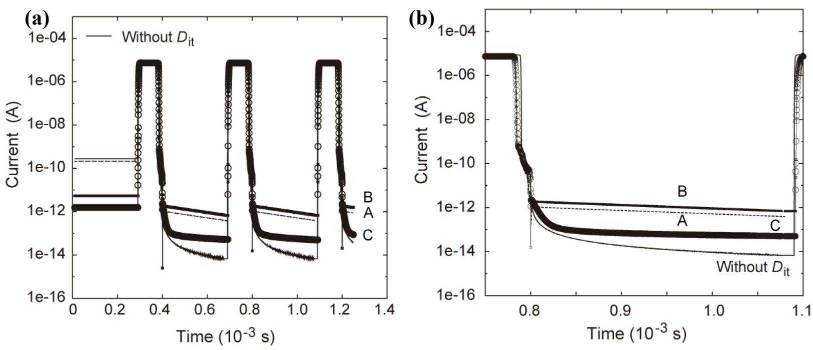

Fig. 4(a). Log plot of the transient collector current during off-state at different cross-section conditions. (b) Enlarged part of the tails currents at off-state.

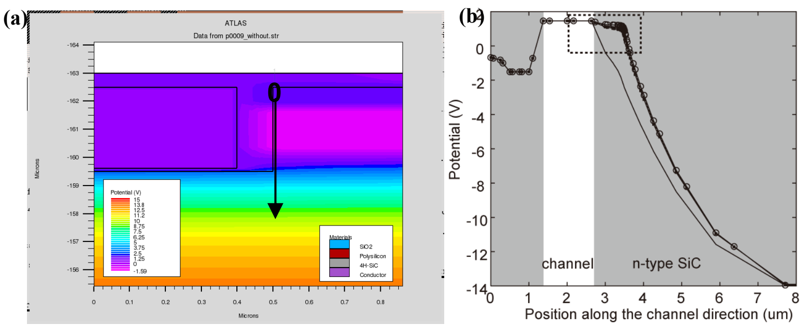

Fig. 5. Potential profile at the channel during off state at different capture cross section conditions. (a) Channel region. (b) Change in potential distribution.

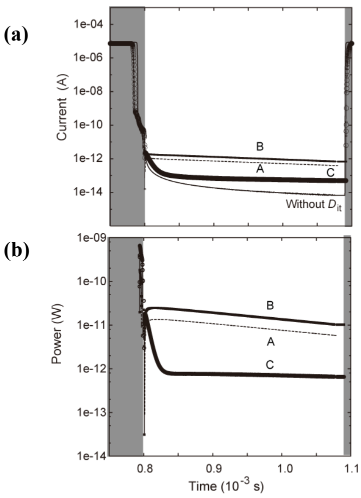

Fig. 6. (a) Calculated current and (b) power dissipated during off-state

Table I. Definition of parameters

Cross section parameter (cm^2)	Defect Distribution	State
SIGTAE (for electrons)	Exponential tail	acceptor-like
SIGTAH (for holes)	Exponential tail	acceptor-like
SIGGAE (for electrons)	Gaussian	acceptor-like
SIGGAH (for holes)	Gaussian	acceptor-like

Table II. Conditions for capture cross-section parameters.

Condition	SIGTAE (shallow)	SIGTAH (shallow)	SIGGAE (deep)	SIGGAH (deep)
A	1.0e-18	1.0e-18	1.0e-18	1.0e-18
B	1.0e-18	1.0e-18	1.0e-14	1.0e-14
C	1.0e-14	1.0e-14	1.0e-18	1.0e-18