Optimization of Etching Paste Process by Screen Printing for Recycling Crystalline Silicon Solar Wafer from End-of-life Photovoltaic Modules

Jeongeun Shin¹ and Jae-seong Jeong^{1*}

¹ Korea Electronics Technology Institute, Robust Components and System Research Center, #25, Saenari-ro, Bundang-gu, Seongnam-si, Gyeonggi-do, 463-816, South Korea Phone: +82-31-789-7052 E-mail: jjseicp@keti.re.kr

Abstract

Deposition of etching paste by screen printing is used for patterning or selective emitter (SE) in solar cell process which activate with SiNx and SiOx. The etching paste process is consist of 3-steps, printing-heating-cleaning. In order to recycle for crystalline silicon wafer, metal electrodes, anti-reflective coating (ARC), emitter, back surface field (BSF) and p-n junction have to remove from the solar cells. In this research, etching paste was applied on front surface of solar cell to remove ARC and emitter at once. Ag and Al metal on both sides of substrate were removed with residue in chemical solution. Deposited etching paste on substrate was treated by different conditions of heating temperature and screen printing. After etching paste process, etching rate was 3~4 nm/s during heating process. All of the needless layers were removed and analyzed by using microwave photoconductance decay (µ-PCD).

1. Introduction

The installed capacity for photovoltaic (PV) system is set to increase continually. At the same time, first PV system have reached the end of their days [1]. PV system has degraded according to temperature, humidity. Aged PV panels are collected and disposed of in incinerators. Manufacturing company have many defective products each process. The defective products use dummy cell and send to scrap company.

Crystalline silicon (c-Si) is one of the most important and valuable materials in PV module and is recoverable from degraded cells [2]. For crystalline silicon solar wafer etching methods were demonstrated through several process as chemical etching, mechanical polishing [2-5]. But, these have not environment friendly, expensive and thickness also not uniformity for manufacturing scale.

In this study, the recycled wafer is achieve by etching paste process. The etching paste is usually investigated for selective emitter highly n^+ doped regions in solar cell process which is easy to apply [6]. When apply etching paste in the recycling process, it can be more uniform surface than any other etching process.

2. Experiment

The experiments were carried out on Czochralski (CZ)

solar grade p-type boron doped mono crystalline silicon conventional solar cell with an area of 156 x 156 mm² (pseudo square), a thickness of 200 μ m. The efficiency for solar cell is 17 %. For re-bare crystalline silicon substrate, all of the layers as metal electrodes, anti-reflective coating (ARC), emitter had to be removed. The process sequence for recycling wafer as shown Fig. 1.



Fig. 1 Process sequence for recycling crystalline silicon solar wafer.

First of all, both side metal electrodes were treated by chemical process. Ag electrode on front surface was removed by using 60 % nitric acid (HNO₃) at room temperature and then Al electrode on rear surface was removed by using 45 % potassium hydroxide (KOH) at 80 °C. The acid (HNO₃) etching step and alkali etching step was conducted for 5 min, 8 min respectively. To remove the ARC and emitter, the etching paste (Solar Etch CES, Merck corp., Germany) which is commercial product is applied. This paste is used widely in industry whereby the etching process was provided only a certain content of phosphoric acid. The etching paste was deposited full size on Ag electrode removed substrate by screen printing method. In order to investigate for effect of heating temperature on the etching rate, the samples were exposed to 5 sorts of maximum of temperature : 320, 340, 360, 380, 400 °C for 2 min through rapid thermal processing (RTP). The remaining etching paste was removed with 0.05 % KOH diluted in deionized water at 50 °C.

3. Results

In the first approach, a removed only front Ag substrate is performed to achieve etching paste. The substrate has contained bowing due to rear side Al contact. Thermal radiation through RTP was not uniform in the substrate and doesn't etched equally. In addition, the Al remained substrate in screen print process has possible cracks on c-Si wafers due to height difference between Al electrode (Al electrode thickness about 20~30 μ m) and wafer surface at edge sides. In the work, all electrodes is removed using acid and alkali solution prior to the open front surface using etching paste. All electrodes were removed on the substrate, thickness of surface had high uniformity during heating process.



Fig. 2 The results of sheet resistance on exposed surface of wafer by etching paste.

Heating temperatures were carried out at 320~400 °C. After 3-steps (printing-heating-cleaning) process, exposed area on the surface of the wafer was measured sheet resistance using 4-point probe. Typically, the etching rate for etching paste is well known about 1~2 nm/s. But the etching rate in this experiment is 3~4 nm/s at 360 °C. Fig. 2 is the 4-point probe results as etched front surface of wafer. This shows that the sheet resistance was observed over 200 Ω/\Box at 360 °C and it means recovered a p-type base substrate.

After final process, minority carrier lifetime of etched c-Si wafer was investigated by microwave photoconductance decay (μ -PCD). Actually, the μ -PCD is use to every process as texturing, diffusion, ARC, metallization in solar cell manufacturing line. Other process as emitter doping, passivation is higher than ~10 μ s. All injected materials were removed by etching process, minority carrier lifetime was demonstrated very low. The bare wafer or textured wafer has value average 1~2 μ s in 6-inch size commercial wafer. The recycled wafer also has average 2.067 μ s lifetime. The range of lifetime of recycled wafer belong to value of the virgin c-Si wafer.



Fig. 3 The result of minority carrier life time mapping of the recycled wafer.

4. Conclusions

In this research, we carried out the etching process through screen printing for recycling silicon wafer. For recycled wafer, Ag and Al metal electrodes were etched by HNO₃ and KOH respectably, and ARC, emitter layer were removed by etching paste at once. The etching rate can be controlled using heating condition, we found that optimized temperature at 360 °C for recycled wafer. Finally we were able to achieve uniform and smooth surface condition. The c-Si wafer has thickness over 160 μ m that can be applied in solar cell production.

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