Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp530-531

Field Test of Dye-Sensitized Solar Cells by utilizing a Power Delivery CMOS Integrated Circuits

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Abstract

Newly developed Power Delivery CMOS Integrated Circuits (PDIC) enables field test of Dye-Sensitized Solar Cells (DSSC) effectively. Quick feedback of failure analysis to the DSSC fabrication and housing process accelerates DSSC for actual use.

1. Introduction

Recently, a Dye-Sensitized Solar Cell (DSSC) has been intensively being investigated, because of its low fabrication cost, shape flexibility and less environmental damage. One of the most suitable applications is wearable battery charger for mobile devices[1)]. But, for aiming the actual use, mass data taken in a field work is necessary, focusing on the total performance of the DSSC power generation system, based on individual device one. This paper proposes a DSSC testing methodology by using newly developed Power Delivery CMOS Integrated Circuits (PDIC).

2. PDIC Concepts

The block diagram of the PDIC is shown in Fig. 1. In order to prevent the reverse leakage current toward a DSSC in inactive state, the PDIC utilizes transfer-gates, working as a switch. The voltage drop of the transfer-gate depends on the current flow, but it can be designed to be negligibly smaller by enlarging the transistor width. As a result, it is possible to collect the electric power even in a parallel connection of low voltage power generating device, and to store the summation of a power on a capacitor. The power generating condition of each DSSC is stored in a FlipFlop, by comparing the DSSC's output voltage with a reference voltage (*Vref*).

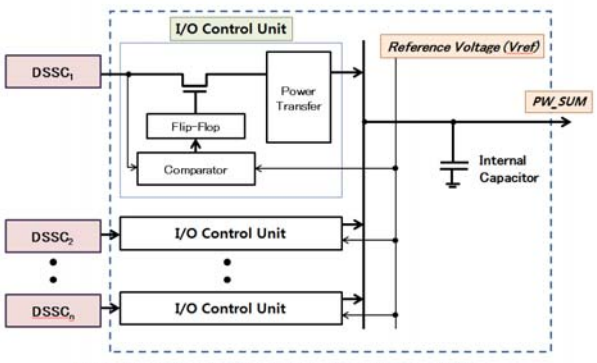

Fig. 1 Block Diagram of PDIC. "n" means the number of DSSC.

Figure 2 shows the chip layout of the PDIC. It was fabricated by a 0.18um CMOS process. Up to 64 DSSCs can be connected.

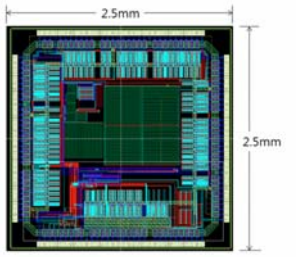

Fig. 2 Chip Layout of PDIC.
64 DSSCs can be connected at the maximum.

3. DSSC fabrication

The structure of a hand-made DSSC is shown in Fig. 3. It consists of TiO_2 film deposited on FTO, together with dye-A or dye-B, and electrolyte. The counter electrode is made of platinum film. Electric contact between the TiO_2 particles was produced by sintering with sophisticated temperature ramping sequence. The DSSC is exposed by the light through 0.28cm^2 hole area.

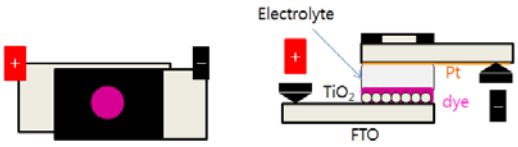

Fig. 3 Structure of DSSC

4. Measurement Results in Field Test

16 DSSCs were fabricated and connected in parallel to the PDIC's 16 I/O Control Units, and we started field test as shown in Fig.4.

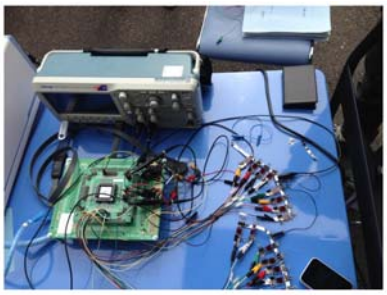

Fig. 4 Field Test

The PW_SUM (Power Summation) wave form with load is shown in Fig. 5. In the Figure, at first all the DSSCs are disconnected, and then these are connected one by one to the PW_SUM node. If the load

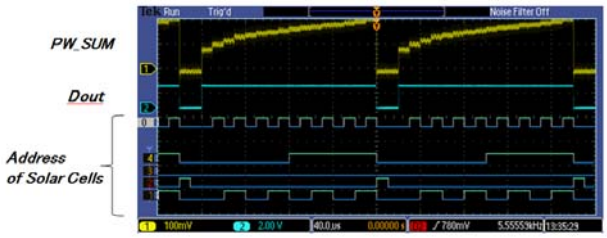

Fig. 5 PW_SUM wave form with 100Ω load

impedance of PW_SUM is high enough, the voltage reaches the inherent voltage rapidly, but if the impedance is low, the wave form looks like stairs as shown in Fig. 5. It means that the PDIC, collecting the power of DSSCs, works properly as designed.

The signal '*Dout*' in Fig. 6 reveals an active or inactive state of each DSSC without load. If *Dout* is high, the corresponding DSSC is active, meaning it is generating a power, whose voltage is above *Vref*. If the performance variation among DSSCs exists, by setting *Vref* higher, the number of active cells decreases. If *Vref* is 600mV, only 6cells are active. The active state is changed by the lightning condition depending on the weather, and the degradation of a cell. They can be detected in real time.

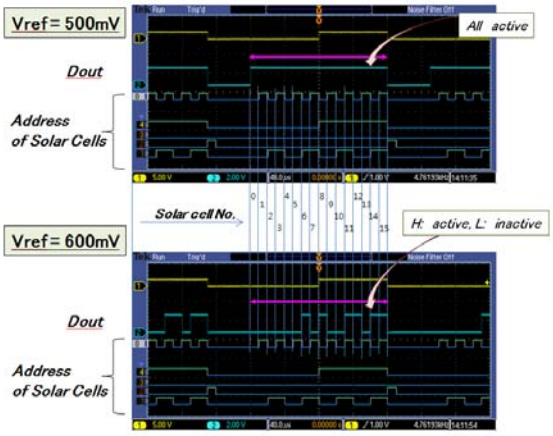

Fig. 6 active or inactive cells, dependent of Vref

The PW_SUM current degradation dependence on days as a function of the output voltage is shown in Fig. 7. The output current depends on the output voltages, shown above the Figure. Under the current fabrication and housing condition, the PW_SUM output current decrease almost half after a month lasts.

By changing *Vref*, the open-circuit-voltage (VOC) of each cell can be monitored. Figure 8 show the VOC variation among cells, on initial and a month later. The DSSC with Dye-B shows better performance than one with Dye-A.

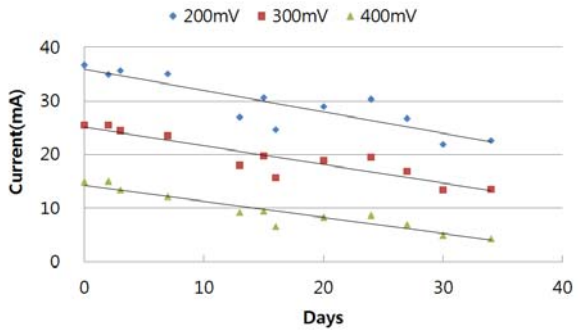

Fig. 7 PW_SUM current as a parameters of output volatages

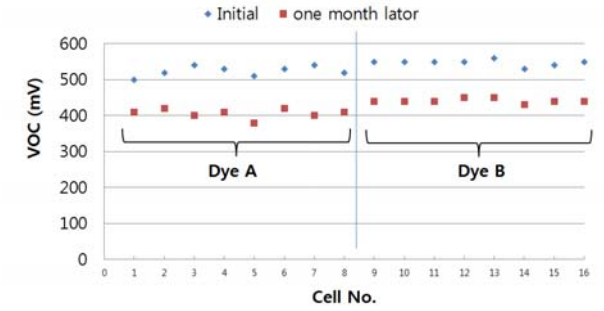

Fig. 8 VOC variation among 16DSSCs

Figure 9 depicts the variation of short-circuit current (ISC).It also degrades after a month. The ISC degradation is larger than that of VOC.

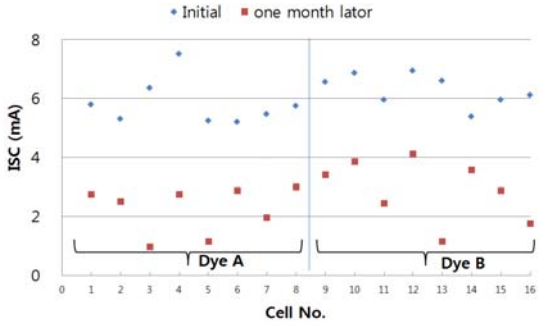

Fig. 9 ISC variation and degradation as a functions of Dye

5. Discussions and Conclusions

By using newly developed PDIC, numbers of DSSC characteristics in a field are taken effectively. It makes possible to carry out many trials by changing fabrication and housing process. The short turn-around time will accelerate the DSSC optimization for actual use. The testing methodology using PDIC is applicable not only to the DSSC but to Organic Solar Cells and thermo-element converters.

Acknowledgement

This work is supported by Chubu University Research Fund, and VDEC (VLSI Design and Education Center), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

References

1) http://paulinevandongen.nl/projects/wearable-solar-shirt/