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Discrete Dopant Impact on the 7 nm Nanowire Transistor Performance

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Abstract

We present a simulation study of discrete dopant charge impact on the performance of a generic 7-nm nanowire transistor. Firstly the Drift-Diffusion (DD) simulation deck coupled with density gradient (DG) correction is shown to be valid by calibration to 2D Schrodinger quantum simulations and ensemble Monte Carlo transport simulations. Then the discrete acceptors in the n-channel of nanowire transistors are introduced and simulated, and the impact of discrete dopant charges on the nanowire performance including threshold-voltage and drive current are investigated.

1. Introduction

Driven by progressive scaling-down of transistors and performance requirements, tri-gate FinFET architectures have already been introduced at the 22 nm technology generation [1]. Multi-gate architectures enable better electrostatic integrity and less statistical variability due to their tolerance of low channel doping [2]. However, the leakage current in the sub-fin region requires punchthrough stoppers. High doping implantation cannot completely eliminate leakage, and use of a buried oxide increases the material cost. Therefore, the gate-all-around nanowire transistor (NWT) structure is proposed for the 7nm technology and beyond [3][4]. In this paper we will show that the 7 nm nanowire transistor performance can be accurately simulated using the GSS TCAD simulation tool coupled with 2D Poisson-Schrodinger solution and ensemble Monte Carlo transport simulations [5]. As variability is a big concern to nanoscale transistor performance, the impact of discrete dopant effects are investigated in this paper to show how it significantly affects the device performance.

2. Nanowire transistor and Simulation Calibrations

We study an elliptical cross-section nanowire transistor although the cross-section shape varies subject to manufacturing processes [3][4]. Fig. 1 illustrates the simulation domain. It features an 8×7 elliptical cross-section, 18 nm gate-length, and interfacial layer/high-k oxide with metal gate. The channel is aligned along the <110> orientation on a (001) wafer. The channel is undoped and source/drain regions are doped with n-type doping of 2×10^{20} cm^{-3}.

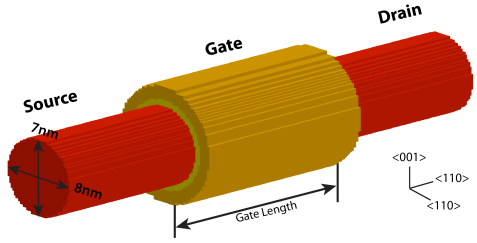


Fig. 1 The simulation domain of a nanowire NFET.

The GSS device simulation tool Garand is at first calibrated by the coupled 2D Poisson-Schrodinger (PS) solution over the channel cross-section. The charge distribution in the channel is matched by adjusting the effective masses of the density-gradient quantum correction, as shown in Fig. 3. Then, the transport in the DD module is calibrated to ensemble Monte Carlo (EMC) simulations to match the average velocity along the device length at select biases by tuning mobility models. The calibrated I_D-V_G characteristics are shown in Fig. 3.

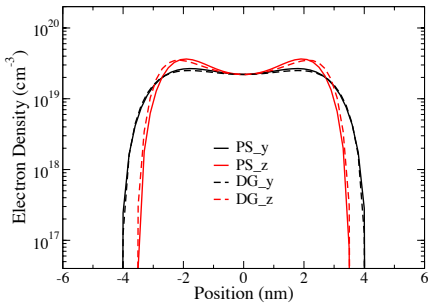


Fig. 2 The DG effective mass calibration of the DD module over 2D cross-section charge distribution, using PS as target. V_G=0.65V.

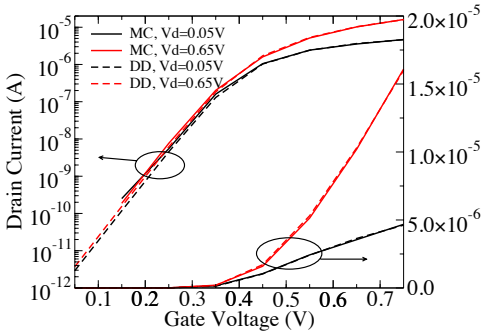


Fig. 3 The calibration of I_D-V_G characteristics against EMC simulation results.

3. The impact of discrete dopant charge

Among the many sources of local variability, discrete dopants in the channel are consistently the major statistical variability source. In this study we intentionally introduce a single acceptor dopant charge into the n-channel NWT, and by varying the dopant location we investigate how it affects NWT performance. At first, a discrete dopant is placed in the middle of the channel, and PS simulation is employed. The negatively charged acceptor results in a potential peak in the middle, which changes the quantum well. The 2-fold (Δ2) valley is the preferentially populated valley in silicon for this orientation, and the charge distributions in the first four subbands are compared, as illustrated in Fig. 4. Firstly, the electrons are distinctly distributed in the subbands, and the presence of the acceptor dopant reduces the magnitude

of all distributions. Secondly, the distributions of subband 1 and subband 4 are changed due to the presence of the dopant. Therefore, in general terms the acceptor dopant reduces the electron density in the channel. Thereafter, the calibrated DD module simulated electron densities in two cases are compared as shown in the last row of Fig. 4. Due to a short vertical radius the on-state electrons crowd near the top and the bottom in the cross-section. The acceptor caused large reduction of electrons is accurately captured in DD module.

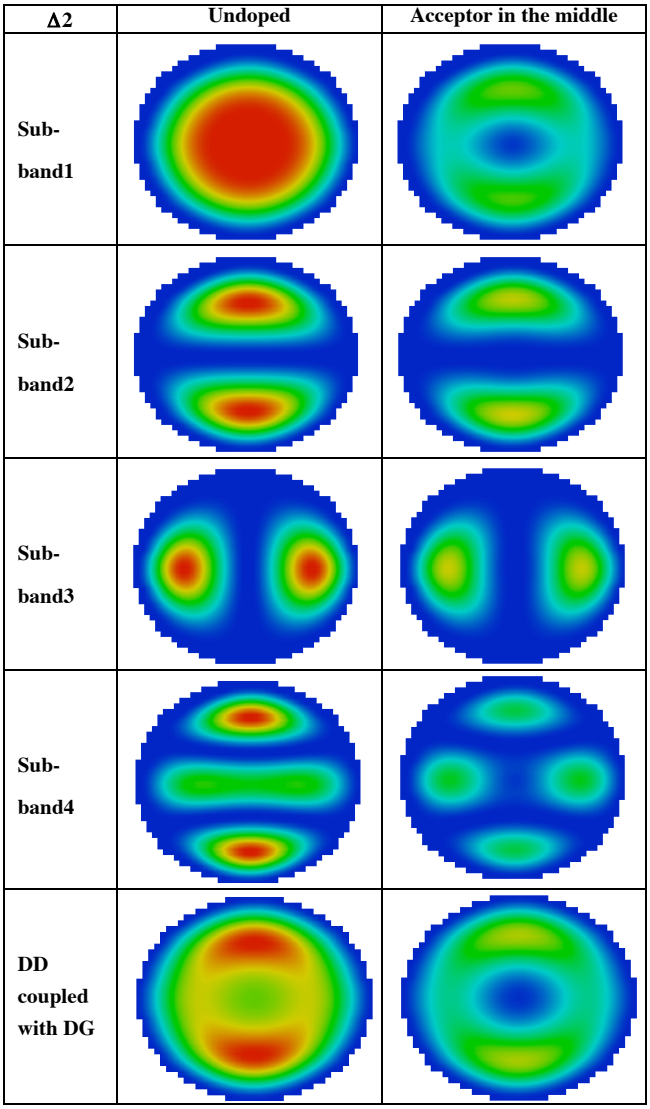


Fig. 4 The degenerate Δ2 valley first 4 subband charge density response and DD (coupled with DG) simulated electron density response to an acceptor (negative) dopant charge in the 8x7 elliptical channel. V_G=0.65V.

The discrete dopant charge effect on the NWT electrical characteristics is investigated using the calibrated DD module. The presence of the negative dopant charge in the nFET channel increases the threshold voltage (V_T) and reduces the current. By varying the dopant position in the channel we have examined the threshold voltage response. It is clear in Fig. 5 that the threshold-voltage response to the dopant located in the channel cross-section renders a bell-shape, and the most sensitive region is in the middle of channel. The largest threshold-voltage change (ΔV_T) approaches 41 mV. The bell-shape will change accordingly with cross-section variation, but the most sensitive region is located in the middle due to the large charge distribution confined by the quantum barrier.

The effect of the position of dopant along the channel is also examined shown in Fig. 6(a). Here 0nm represents the middle of channel with the source to left and drain to right. In the case of simulations at low drain bias, the threshold voltage shift due to a dopant increases as it moves from source end towards the middle, and reaches the largest value of 35mV in the middle of channel before decreasing towards the drain side. This is attributed to electron distribution along channel with the largest electron density in the middle. In the case of high drain bias, the highest electron density shifts towards the source side, and therefore, the large ΔV_T shifts towards the source side.

The drive current response to a discrete dopant in the channel is also studied, as shown in the Fig. 6(b). It is clear that on-current reduction due to an acceptor along the channel can reach up to 12% just beyond middle.

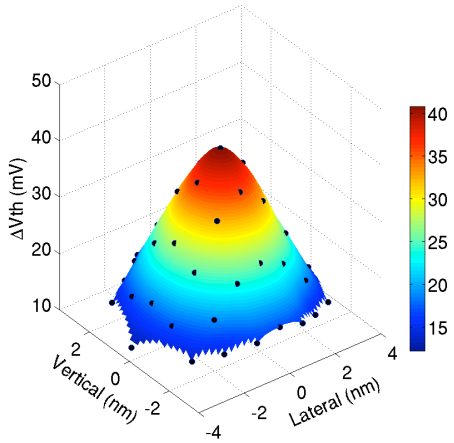
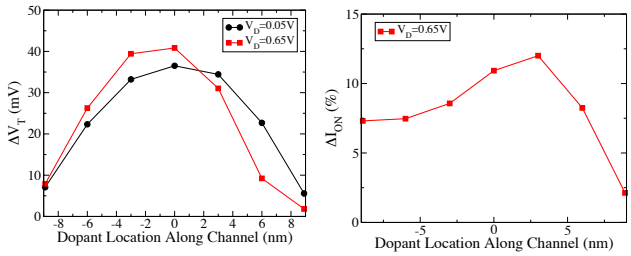


Fig. 5 The threshold voltage change due to a doped acceptor in the channel cross-section of the n-channel nanowire transistor.



(a) (b)

Fig. 6 The sensitivity of threshold voltage (a) and drive-current reduction (b) to discrete dopant (acceptor in n-channel) location along channel.

4. Conclusions

In this abstract we investigated the impact of single dopant effects on the performance of a 7nm NWT using DD simulations coupled to Poisson-Schrodinger solutions and calibrated to Monte Carlo simulations.

Reference

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