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Impacts of Threshold Voltage Design for Monolithic 3D 6T SRAM with Si and InGaAs-n/Ge-p Devices considering Interlayer Coupling

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Abstract—For high performance operation, TCAD results indicate that 6T SRAM cell with high threshold voltage (V_T) design exhibits larger static noise margin (SNM), lower leakage but lower performance compared with low V_T design. However, monolithic 3D structure with optimized 3D layout can improve SNM and reduce the gap in performance for high V_T design. Furthermore, monolithic 3D InGaAs-n/Ge-p SRAM with high V_T design offers enhanced performance with comparable SNM with the Si counterpart.

1. Introduction

3D integration is crucial to improving chip density, reducing interconnect delay and enabling heterogeneous integration. Among various 3D technologies, monolithic 3D integration, which stacks multiple layers sequentially, facilitates ultra-fine inter-tier vias and short interconnection [1-2]. The implementations of two-tier monolithic 3D inverter using Si-n/Si-p and InGaAs-n/Ge-p devices have been successfully demonstrated [1][3]. With thin interlayer dielectric (ILD), the increasing interlayer coupling may alter the characteristics of upper-tier devices, and offer the opportunity for optimization of monolithic 3D circuits [4-6].

Embedded SRAM occupies substantial portion of SoC area. For high performance 2D 6T SRAM operating at high V_{DD}, high V_T SRAMs show better variation immunity while sacrificing performance compared with low V_T design [7]. Besides, monolithic 3D 6T SRAMs composed of Si/Si (NMOSFET/PMOSFET) and InGaAs/Ge with interlayer coupling can improve cell stability and performance simultaneously through optimized 3D layouts [8]. In this work, we further investigate cell stability and performance of monolithic 3D 6T SRAM under variable V_T designs while considering interlayer coupling.

2. Monolithic 3D Structure and TCAD Methodology

We consider monolithic 3D structure with two-tier layer design, one for NMOSFET and the other for PMOSFET (Fig. 1). With interlayer coupling, the front gate of the bottom-tier transistor provides a dynamic or fixed back-gate bias (V_{bg}) for the upper-tier device.

This work investigates 3D SRAMs under different tier combinations ((Upper/Bottom) tier for (N/P) and (P/N) MOSFET) and possible layouts. Based on physical layouts, three possible layouts depending on the gate alignment are listed below: (1) PG-PU (PU-PG), (2) PD-PU (PU-PD), (3) PD-PU, PG-$V_{L(R)}$, where PU, PD and PG represent Pull-Up, Pull-Down and Pass-Gate device in 6T SRAM cell, respectively [6].

For comparison, planar 2D 6T SRAM with two back-gate biases (V_{bg} = 0V and V_{bg} = V_{DD} for NMOSFET and PMOSFET, respectively) is adopted as the base 2D design. In other words, the 2D SRAM has zero body-to-source bias. The back-gate biases of 3D SRAM depend on different tier combination and layout. The global bottom-tier V_{bg} of 3D 6T SRAM is adaptive for different operation modes for better stability and performance. During Read mode, forward-biased PMOS for (N/P) tier (or zero-biased NMOS for (P/N) tier) is utilized, and zero-biased PMOS (or forward-biased NMOS for (P/N) tier) is used at Write mode (Table. 1). It shows that monolithic 3D structure can exploit V_{bg} to offer another degree of design freedom without area penalty.

TCAD mixed-mode simulations [9] are performed considering the interlayer coupling of monolithic 3D 6T SRAM. The device parameters of calibrated ultra-thin-body (UTB) SOI are listed in Fig. 1. Fig. 2 shows the Ids-Vgs characteristics of UTB SOI devices with high/low V_T design (high V_T equals to 0.4V while low V_T equals to 0.2V), under zero and forward body-to-source bias.

3. Results and Discussion

2D 6T SRAMs with high V_T design show larger read static noise margin (RSNM) compared with the low V_T counterparts (Fig. 3). The RSNM improvement of high V_T design over low V_T design is also shown as the black square in Fig. 4. For all scenarios of 3D SRAMs with interlayer coupling, the RSNM improvement of high V_T design over low V_T design are positive and larger than 2D results (Fig. 4). Among all the 3D scenarios, (N/P) PD-PU, PG-$V_{L(R)}$ has the largest RSNM improvement over low V_T counterpart. However, the WSNM improvement of high V_T design over low V_T counterpart is negative for most of the 2D and 3D scenarios due to the weaker PG (Fig. 5).

The cell leakage of 2D SRAM with high V_T design is more than 2 orders smaller than the low V_T counterpart for all V_{DD} (Fig. 6). The leakage of (N/P) PD-PU, (P/N) PU-PD and (N/P) PD-PU, PG-$V_{L(R)}$ are equal to the 2D results. But (N/P) PG-PU and (P/N) PU-PG exhibit larger cell leakage since one side of the upper-tier off state PG and PU suffer from the dynamic forward-bias from the bottom-tier device, respectively.

For SRAM cell performance analysis, the bit-line loading is estimated based on actual layouts with 64 cells per bit-line. The SRAM cell Read access time is defined as the time from activation of the word-line to when the bit-line differential voltage reaches 10% V_{DD}. The cell Time-to-Write is defined as the time from activation of the word-line to when the storage node voltages crossover.

2D SRAM with high V_T design has slower Read access time and Time-to-Write (Fig. 7, Fig. 8). However, monolithic 3D SRAM with proper back-gate bias can improve the performance for both high/low V_T designs. 3D high V_T SRAM exhibits larger performance enhancement compared with low V_T counterpart because higher V_T device exhibits larger back-gate bias efficiency. Consequently, the performance gap between high/low V_T SRAMs can be further reduced.

For high V_T SRAM, replacing Si/Si CMOS with InGaAs/Ge high mobility channel CMOS can further improve SRAM cell performance. Fig. 9 shows the Ids-Vgs characteristics of calibrated InGaAs-n/Ge-p UTB MOSFETs [10-11], which have V_T equal to 0.4V. InGaAs/Ge SRAMs exhibit faster Read access time and Time-to-Write compared with Si/Si counterparts for 2D and 3D cases (Fig. 10, Fig. 11) while maintaining comparable RSNM and larger WSNM (Fig. 12). The inset of Fig. 10 shows the Read access time improvement of InGaAs/Ge over Si/Si counterparts for 2D and 3D (N/P) PD-PU, PG-$V_{L(R)}$. The improvement of 3D results is more than 40%, which is larger than the maximum improvement of 2D results, due to the forward back-gate bias of PG. However, InGaAs/Ge SRAMs show larger cell leakage compared with Si/Si counterparts due to band-to-band tunneling leakage (Fig. 13).

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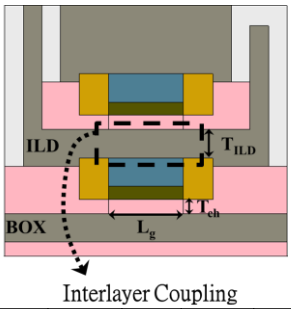

L_g	EOT	T_{ch}	T_{ILD}	T_{BOX}
25nm	0.7nm	5nm	10nm	10nm

Fig. 1. Schematic of two-tier monolithic structure showing the interlayer coupling between tiers.

Table 1. Body-to-source bias (V_{bs}) of the bottom tier devices for 3D 6T SRAM at Standby, Read and Write operation mode.

Vbs_bottom	(N/P)	(P/N)
Standby	Zero bias	Zero bias
Read	Forward bias	Zero bias
Write	Zero bias	Forward bias

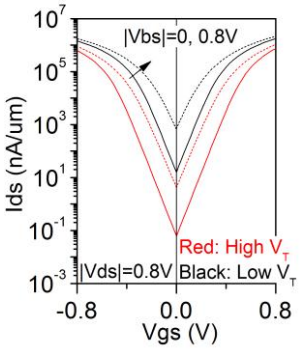

Fig. 2. Ids-Vgs curves of UTB SOI devices with high/low V_T design under zero and forward body-to-source bias.

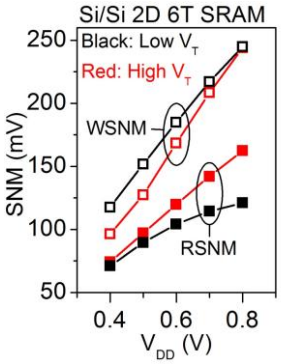

Fig. 3. RSNM and WSNM of Si/Si 2D 6T SRAMs with high/low V_T design versus V_{DD}.

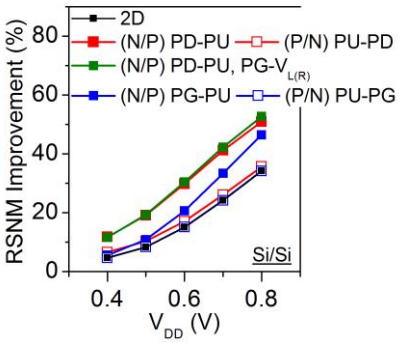

Fig. 4. RSNM improvement of high V_T designs over low V_T counterparts for 2D and 3D Si/Si SRAM scenarios.

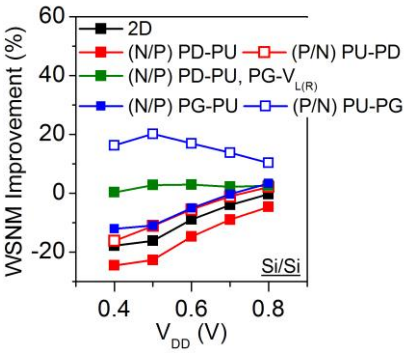

Fig. 5. WSNM improvement of high V_T designs over low V_T counterparts for 2D and 3D Si/Si SRAM scenarios.

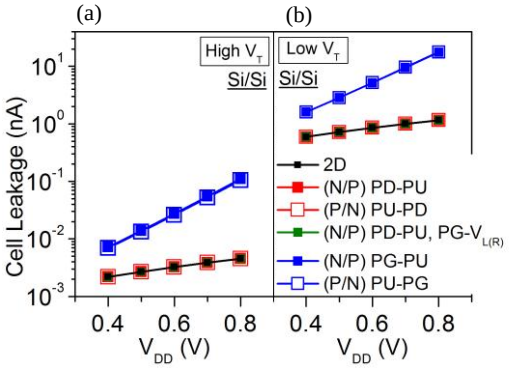

Fig. 6. 6T SRAM cell leakage comparison of (a) high V_T and (b) low V_T design for 2D and 3D Si/Si SRAM scenarios.

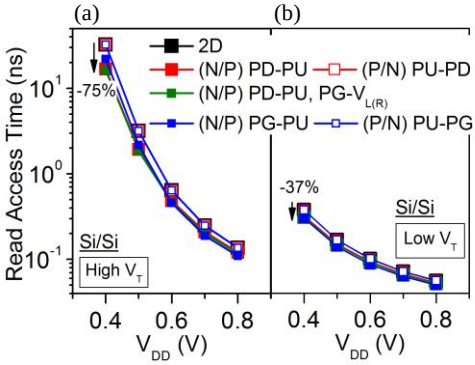

Fig. 7. Cell Read access time of (a) high V_T and (b) low V_T design for 2D and 3D Si/Si SRAM scenarios.

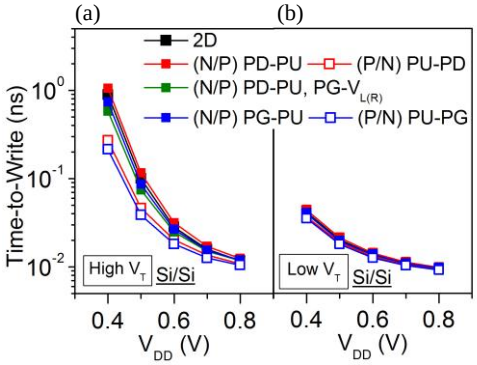

Fig. 8. Cell Time-to-Write of (a) high V_T and (b) low V_T design for 2D and 3D Si/Si SRAM scenarios.

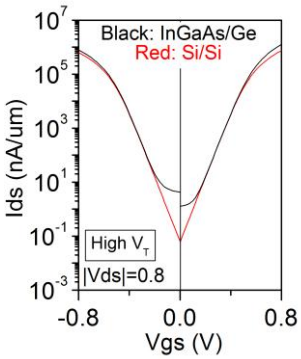

Fig. 9. Ids-Vgs curves of UTB InGaAs-OI/Ge-OI and Si/Si with V_T = 0.4V.

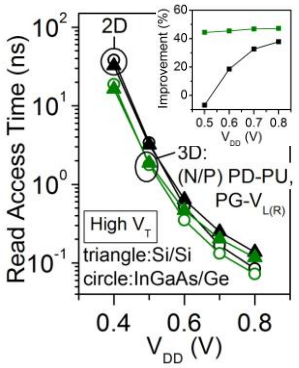

Fig. 10. Cell Read access time of InGaAs/Ge and Si/Si SRAMs for 2D and 3D SRAM scenarios. The inset shows the Read access time improvement of InGaAs/Ge over Si/Si counterparts for 2D and 3D results.

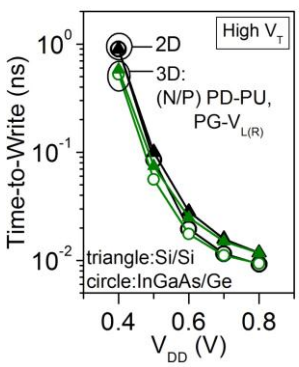

Fig. 11. Cell Time-to-Write of InGaAs/Ge and Si/Si SRAMs for 2D and 3D SRAM scenarios.

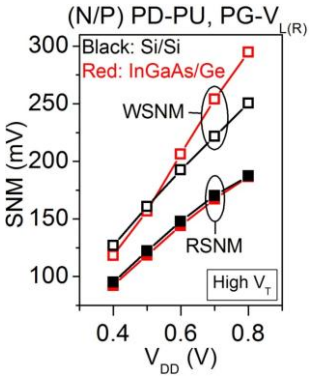

Fig. 12. RSNM and WSNM of 3D (N/P) PD-PU, PG-$V_{L(R)}$ Si/Si and InGaAs/Ge 6T SRAM.

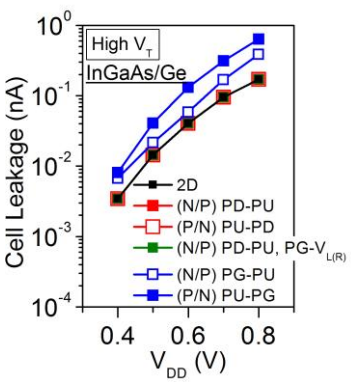

Fig. 13. Cell leakage of high V_T InGaAs/Ge SRAM for 2D and 3D scenarios.