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Multi-Threshold Voltages in Ultra-thin-body Devices by Asymmetric Dual-Gate Structure

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Abstract

Control of threshold voltage (V_T) by asymmetric dual-gate structure is investigated. It is fabricated through two-step chemical mechanical polishing (CMP) processes. V_T of the device is determined by how many charges are trapped in the nitride layer. Additionally, the efficiency of this technique is analyzed by simple capacitance network. It is noteworthy that this method can be used without ultra-thin box structure.

1. Introduction

Ultra-thin body (UTB) devices are promising candidates in deep sub-100 nm regime due to good controllability of short-channel effect and suppression of random dopant fluctuation [1-2]. However, it is hard to realize multi-threshold voltages (V_T) and dynamic V_T modulation with an undoped channel in UTB structure, so there are several techniques to control V_T such as ground plane, back-biasing and multiple gate materials [3-8].

In this study, we propose a new method to control V_T in UTB devices using asymmetric dual-gate structure which is fabricated through two-step CMP processes. It is possible to modulate V_T by trapping charges in the 2nd gate (G2) stack. Furthermore, the impact of body thickness on this method is analyzed.

2. Results and Discussions

Device Concept and Fabrications

The schematic diagram of the proposed device is described in Fig. 1. Structurally, the asymmetric dual-gate is the great feature of the device. Each gate performs a switch of channel and V_T modulation respectively. V_T of the device is strongly reliant upon how many charges are trapped in the G2 stack. Positive charges in the nitride layer shift transfer curves to the left, whereas negative charges shift them to the right.

The fabrication sequence follows the process flow as shown in Fig. 2. First, a hard mask stack is deposited and active patterns are etched. After forming the 1st gate (G1) stack, CMP process is done. 50nm-thin sidewall is formed through deposition and dry etch process of LPCVD-MTO. Then, a silicon fin is formed using dry etch process. The fin is achieved through HBr plasma etch process and its width is defined almost the same as the thickness of oxide sidewall.

After the fin formation, the G2 stack comprised of oxide / nitride / oxide (3 nm / 7 nm / 9 nm) / doped poly-silicon is deposited over the fin and the G1 using LPCVD. The CMP process makes a difference in the thickness of doped poly-silicon and this difference separates two gates by dry etch-back process. Figure 3 which is a cross-sectional scanning electron microscope (SEM) image of the fabricated device shows that these two gates are successfully separated.

Electrostatic Behaviors

Five programming pulses of 15 V and 10 μs are applied to G2 for trapping charges in the nitride layer by FN tunneling. Figure 4 shows measured transfer characteristics of both G1 and G2 as a parameter of programing pulses. It is found that V_T for both gates is changed by the number of trapped charges in the nitride layer. V_T is increased as the programming pulses are applied. About 0.61 V of V_T window for G1 is achieved by five programming pulses as shown in Fig. 4(a), whereas about 4.83 V of V_T window for G2 is achieved for same programming conditions as shown in Fig. 4(b). V_T can be controlled by modulating conditions of programming pulses.

Considering simple capacitance network model as shown in Fig. 5, coupling ratio between these V_T windows is given by

$$Coupling\ Ratio = \frac{C_{\text{nitride}} \,||\, C_{\text{gox2}} \,||\, C_{\text{body}}}{C_{\text{gox}}} \qquad (1)\ .$$

It represents the effect of trapped charges on the channel potential and V_T for G1. The coupling ratio for our fabrication conditions is calculated as 0.129 which is almost the same as measured data 0.61 V / 4.83 V. Figure 6 shows coupling ratio as a function of body thickness. The thinner body thickness, the higher coupling ratio is achieved. To put it another way, this method is much more efficient in UTB structure.

The effect of charges in the nitride layer on channel potential is investigated using simulated energy band contours for same structural conditions as shown in Fig. 7. Understandably, channel potential is far more lessened when the nitride layer is negatively charged compared with when it is neutral. Consequently, this brings out modulation of V_T for G1.

3. Conclusions

A new method of V_T modulation in UTB devices was proposed. It could have multi-V_T by trapping charges in G2 stack which was independent of G1 due to structural feature of asymmetric dual-gate. This method was more efficient at thinner body thickness by capacitance network. It was noteworthy that it could be used without ultra-thin box and V_T could be modulated even after fabrication process.

Acknowledgements

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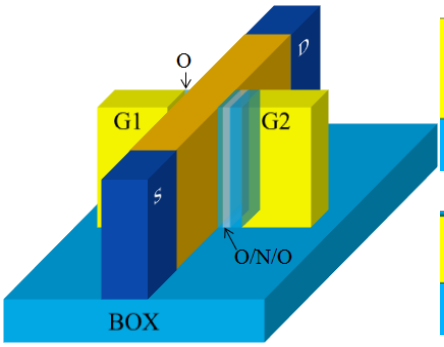

Fig. 1 Structure of the asymmetric dual-gate device.

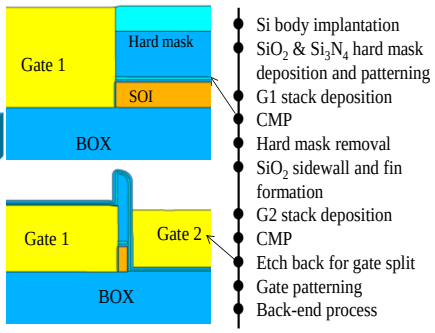

Fig. 2 Fabrication process flow of the asymmetric dual-gate structure.

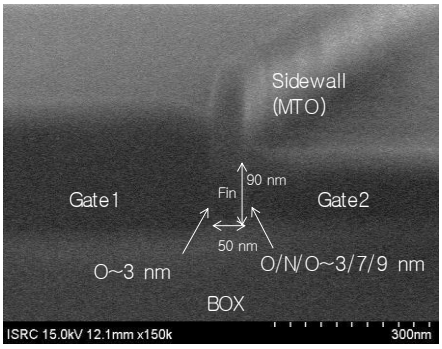

Fig. 3 Cross-sectional SEM image of the fabricated device

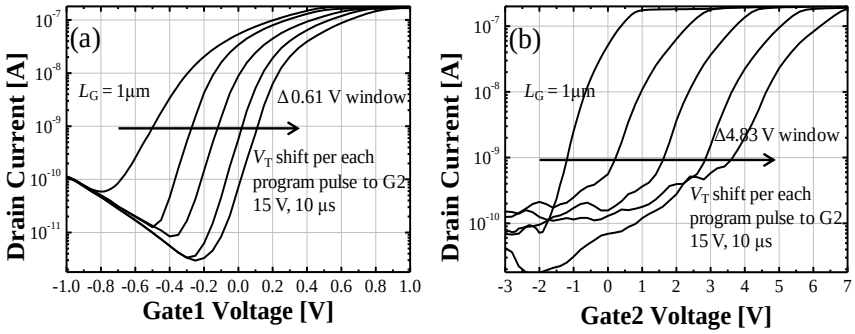

Fig. 4 Measured (a) I_D-V_{G1} curves and (b) I_D-V_{G2} curves of the device with V_D = 1 V as a function of programming pulses.

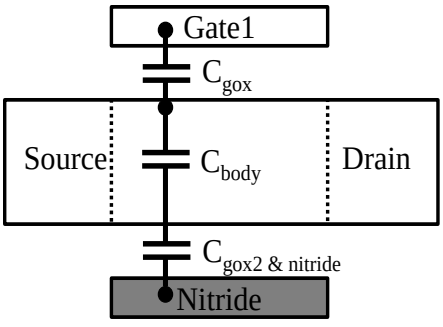

Fig. 5 Simple capacitance network model in the device.

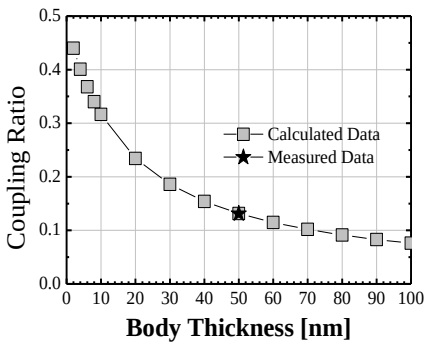

Fig. 6 Body thickness dependence on coupling ratio between ΔV_T for G1 and G2.

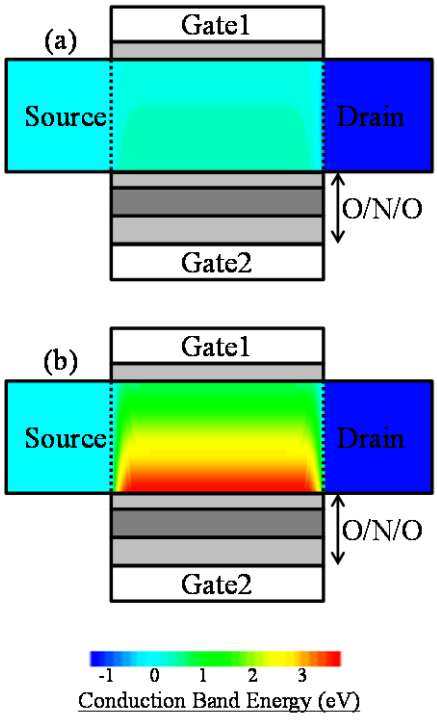

Fig. 7 Contours of conduction band energy with V_G= 0 V and V_D = 1 V when nitride layer is (a) neutral and (b) negatively charged.