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Investigation of trap properties in High-k/Metal Gate pMOSFETs of Higher Al Energy and Concentration Ion Implantation on Random Telegraph Noise

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Abstract

In this study, the impact of aluminum ion implantation (Al I/I) with different energy and doses on random telegraph noise (RTN) in high-k/metal gate (HK/MG) p-type metal–oxide–semiconductor field-effect transistors (pMOSFETs) was investigated. The Al I/I can reduce oxide trap densities, because the Al filled the defects and formed a thin Al_2O_3 layer. However, when energy and doses increased, higher Al concentration will cause gate tunneling current density (J_G). In addition, in the RTN, we were also observed that the trap position (X_T) in the control device was lower, maybe due to Al not diffusion too deeply near SiO_2/Si interface.

1. Introduction

Random telegraph noise (RTN) is a special kind of g-r noise occurred at the range of low frequency. RTN originates from the trapping/detrapping behaviors of a single trap, resulting in the phenomena of two discrete current levels in the time domains and is believed as a good approach to study the individual defect properties in small-area MOSFETs (1 μm^2 <). It is known that RTN can be used to monitor distributions and characteristics of oxide traps. Thus, RTN should be an effective tool for studying individual defect behavior via carrier capture and emission, which in turn, should be beneficial for the development of new process flows. As the continued shrinking of conventional CMOS devices, the suppression of higher gate leakage current owning to decreasing gate oxide thickness has emerged as a key technology for improving device performance [1]. For the sub-28-nm era, issues such as direct gate tunneling, poly-gate depletion, gate sheet resistance, boron penetration, and Fermi level pinning [2] all become severe obstacles to the improvement of device performance. To overcome these obstacles, HK materials and MG electrodes have been used to replace conventional SiO_2 gate oxide and poly-gate electrodes, respectively. Hafnium (Hf) based high-k stacks have an attraction for replacing SiO_2 as the insulator of metal-oxide-semiconductor field-effect transistors (MOSFETs) due to the high permittivity, appropriate band gap (E_G), and good thermal stability with Si. However, fabricating MG pMOSFETs with a low threshold voltage (V_T) and with a small equivalent oxide thickness (EOT) in particular is still a crucial challenge in gate-first integration owing to the presence of numerous oxygen vacancies and defect sites in the HK gate dielectric [3]. It has been reported that one can employ an Al_2O_3 capping layer to modulate the effective work function (EWF) near the Si valence band edge to meet the V_T requirement of pMOSFETs. However, the use of an Al_2O_3 capping layer often results in increased EOT. Alternatively, to obtain a large V_{FB} shift with a minimal EOT penalty in HK/MG pMOSFETs, aluminum ion implantation (Al I/I) technology was implemented and identified as an effective approach for EWF modulation without increasing the EOT or involving a complex process. In this paper, the use of RTN to evaluate HK/MG pMOSFETs with different energy and doses of Al I/I was investigated. The effects of employing Al I/I on trap properties, such as activation energy, capture and emission kinetics, and spatial depth from the channel of HK/MG pMOSFETs, were investigated by temperature-dependent RTN.

2. Device Structure and Experiment

The Al I/I pMOSFETs used in this study were all fabricated using 28-nm gate-first HK/MG technology CMOS process are illustrated in Fig. 1. The gate dielectrics consisted of a ~1-nm-thick thermally grown SiO_2 interfacial layer (IL) and a ~2.5-nm-thick HfO_2 film prepared by atomic layer deposition. A 10-nm-thick TiN layer prepared by radio-frequency physical vapor deposition was then deposited on top of the gate dielectrics. The Al I/I was subsequently performed through TiN following gate metal deposition with implantation energy of 1.2 keV and dose of 5×10^{15} cm^{-2} is control device, at 1.5 keV with a dose of 5×10^{15} cm^{-2} and 1×10^{16} cm^{-2} for devices A and B, respectively. To avoid singularity effects and demonstrate the reproducibility of the oxide trap characteristics, three devices were measured to determine the device-to-device variation and ensure that the results are reproducible [4].

3. Results and Discussion

To understand the effects of Al I/I on the trap parameters within HK dielectrics, we measured the RTN characteristics of the all fabricated devices. In the RTN measurement, a distinct difference in I_D between two states under different V_G is observed as shown in Fig. 2 for the control device, devices A, B, respectively, which is responsible for carrier trapping and detrapping at a single trap site and confirms the existence of RTN in all devices. The extracted mean capture time (τ_c) and mean emission time constant (τ_e) as functions of the gate overdrive (V_G - V_T) plot is shown in Fig. 3. It should be noted that small values of τ_c and τ_e indicate that capture and emission events occur very frequently and that a given device has a small trap depth (X_T). The Fig. 3 also shows that τ_c decreases and τ_e increases with the increase in V_G - V_T for all devices. Figure 4 shows the dependence of $\ln(\tau_c/\tau_e)$ on V_G - V_T for the fabricated devices. The X_T from the insulator/semiconductor interface can be extracted using the following formulas [5]:

$$X_{T1} = \left(T_{ox1} + \frac{\varepsilon_{ox1}}{\varepsilon_{ox2}} T_{ox2}\right)\left(\frac{k_B T}{q}\frac{\partial \ln(\tau_c/\tau_e)}{\partial V_G} + \frac{\partial \varphi_s}{\partial V_G}\right)\Big/\left(\frac{\partial \varphi_s}{\partial V_G} - 1\right) \quad \text{.....(1)}$$

$$X_{T2} = \left(T_{ox2} + \frac{\varepsilon_{ox2}}{\varepsilon_{ox1}} T_{ox1}\right)\left(\frac{k_B T}{q}\frac{\partial \ln(\tau_c/\tau_e)}{\partial V_G} + \frac{\partial \varphi_s}{\partial V_G}\right)\Big/\left(\frac{\partial \varphi_s}{\partial V_G} - 1\right) + \left(1 - \frac{\varepsilon_{ox2}}{\varepsilon_{ox1}}\right) T_{ox1} \quad \text{.....(2)}$$

where X_{T1} and X_{T2} are the trap depths for the active traps located within the IL of SiO_2 and within the HK layer, respectively. T_{ox1} and T_{ox2} are the physical thicknesses of the IL and HK layers, respectively. ε_{ox1} and ε_{ox2} are the dielectric constants of SiO_2 and the HK film, respectively. As shown in Fig. 4, the dashed lines represent the linear fitted curves that are used to obtain the X_T values of all devices. The obtained values of X_T are 1.92, 1.75, and 1.51 nm for device B, device A, and the control device, respectively. In other words, the trap in the HK layer was located closer to the IL/Si interface for the control device, than it was for the other both devices. This observation should be attributed to the

fact that the implanted Al could react with oxygen vacancies at the bottom of the HfO_2 layer to form Al–Si–O bonds and thus induce dipoles at the HfO_2/SiO_2 interface. But, when energy and doses increased, higher Al concentration diffusion too deeply near SiO_2/Si interface will accompanied with EOT increasing and cause gate tunneling current density (J_G) performance degradation due to non-optimized implant condition. In addition, Fig. 5 (a) and (b) shows temperature-dependent RTN fluctuations measured for these three devices. τ_c and τ_e decrease as temperature increases. Based on the temperature-dependent RTN results, from Table I we should be able to extract the barrier energy (ΔE_B) for carrier capture, the activation energy ($\Delta E_{TV} = E_T - E_V$) for carrier emission, and the effective capture cross-section (σ_0) of the defect [6]. Here, ΔE_{TV} is defined as the energy difference between the trap level (E_T) in the gate dielectric and the valence band maximum (E_V) in silicon. In other words, ΔE_B decreased by 0.09 eV, whereas ΔE_{TV} increased by 0.11 eV for device B relative to the control device. Based on these values, we can plot a schematic energy configuration-coordinate diagram of the all fabricated devices. As shown in Fig. 6, it was observed that the trap in the control device had a lower energy level (E_T) and was located closer to the IL/Si interface than that in the other both devices. It should be noted that the higher E_T is, the smaller the energy difference ($E_T - E_F$) becomes (i.e., the trap energy level E_T can cross the Fermi level, E_F, easily). Thus, the lower E_T observed for the control device suggests the intersection of the emission and capture times should occur at a large negative gate overdrive, which agrees well with the results shown the Fig. 3. This discrepancy should be attributed to the fact that the implanted Al could fill defects and form a thin Al_2O_3 layer, but excess Al ions accumulated to the SiO_2/Si interface maybe cause J_G, V_{FB} and reliability degradation.

On the other hand, the tunneling barrier height φ_B for holes became smaller, and the tunneling attenuation length for carriers penetrating into the dielectric, λ, became longer. The reduced λ implies a smaller tunneling probability and lower J_G for the control device. The J_G of 1.22×10^{-4}, 1.66×10^{-3} and 8.57×10^{-3} A/cm^2 were obtained for control device, devices A and B, respectively, under bias condition of V_G = -1 V and V_D = Vs = V_B = 0 V shown in the Fig. 7. Smaller J_G of the control device verifies clearly the device has a higher φ_B than that in the other both devices.

4. Conclusions

We investigated the behavior of traps in HK/MG pMOSFETs with Al I/I and different energy and doses using RTN. Although the Al I/I can improve the quality of gate stacks by passivating defects in insulator, higher Al concentration would cause the degradation in J_G owing to the lower φ_B and longer λ for hole, which can be attribution to the accumulation of excess Al at SiO_2/Si interface. More studies must be carried out to optimize the Al profile to minimize the induced worsening of gate leakage by the diffusion of Al too deep into the Si substrate will not lead to deterioration of the reliability and performance.

Acknowledgements

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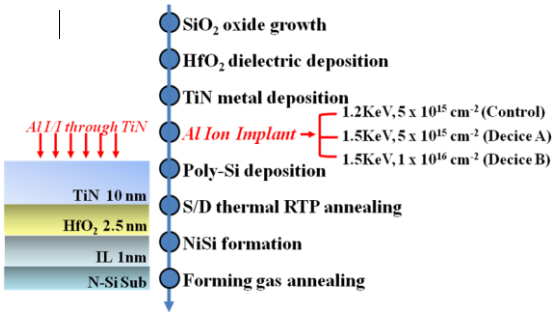

Fig. 1 Schematic of pMOSFET structure with process flow sequences of 28nm HK/MG process.

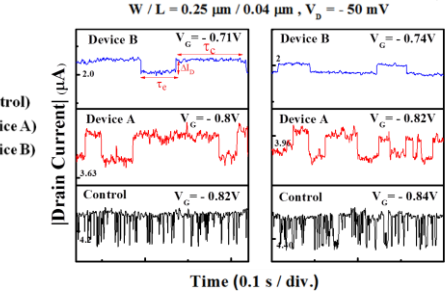

Fig. 2 Room temperatures drain current RTN for all devices with a 40-nm gate length and a 25-nm gate width as function of the gate voltage.

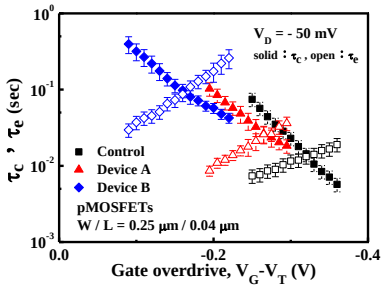

Fig. 3 Comparison of the capture time (solid) and emission time (open) for all HK/MG pMOSFETs.

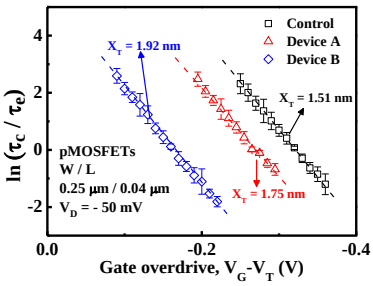

Fig. 4 The dependence of the mean capture time (τc)/mean emission time (τe) with respect to the gate overdrive for all HK/MG pMOSFETs.

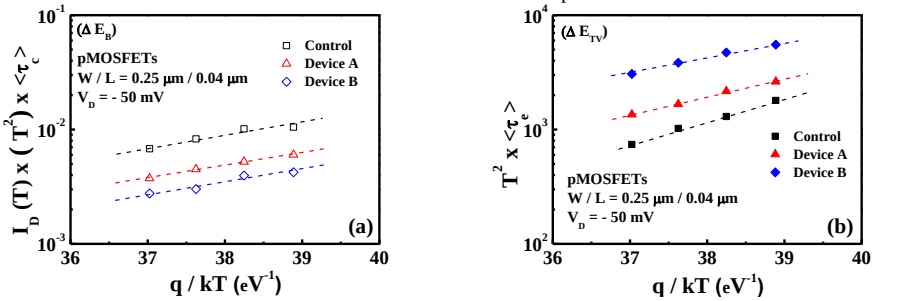

Fig. 5 Temperature dependence of mean capture time (a) and mean emission time (b), as obtained from the RTN fluctuations for all HK/MG devices.

Device	ΔE_B (eV)	ΔE_{TV} (eV)	σ_0
Control	0.33 eV	0.15 eV	3.76×10^{-18}
Device A	0.27 eV	0.22 eV	6.55×10^{-18}
Device B	0.24 eV	0.26 eV	9.33×10^{-18}

Table I. Extracted barrier energy (ΔE_B), trap activation energy ($\Delta E_{TV} = E_T - E_V$), and effective capture cross-section (σ_0) of all devices.

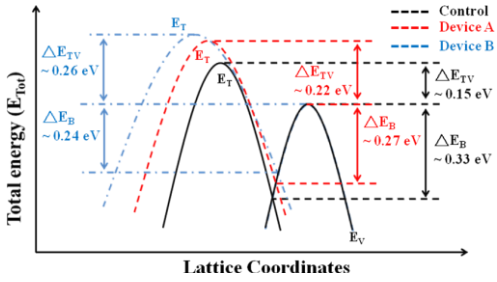

Fig.6 Schematic energy configuration-coordinate diagram showing the changes in total energy of the system as a hole is transferred from the inversion layer into an interfacial defect.

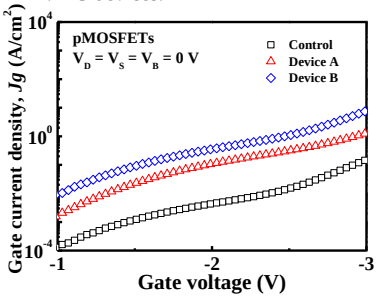

Fig.7 The gate tunneling current (J_G) versus gate voltage (V_G) for all HK/MG devices.