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The Limits of Applicability of the Analytic Model for Hot-Carrier Degradation

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Abstract – We study the applicability of our analytic model for hot-carrier degradation (HCD), which was derived to represent HCD in nLDMOS devices, in the context of planar nMOSFETs. We use devices with different gate lengths of 2.0, 1.5, and 1.0µm. We show that although the model can adequately represent the linear drain current change in the 2.0µm transistor it starts to fail for a gate length of 1.5µm.

1. Introduction

Our physics-based HCD model requires a detailed knowledge about the carriers energy distribution function (DF) as both hot and cold particles can trigger different bond breaking mechanisms such as single- and multiple-carrier processes [1]. It was shown that even in the case of high-voltage devices low-energy particles can play a significant role [2,3]. Thus, a proper description of the DF is inevitable. The DF can be obtained as the exact solution of the Boltzmann transport equation (BTE) and can be provided by means of our deterministic BTE solver which uses the spherical harmonics expansions (SHE) method. However, for devices with high stress/operating voltages and complex geometries, as LDMOS transistors, this can be a complicated and computationally demanding task making the modeling of HCD intricate.

We have recently proposed an HCD model developed for LDMOS devices [3], which uses a simplified analytic expression for the carrier DF based on the moments of the BTE. This model is computationally not expensive since it uses the drift-diffusion (DD) scheme. The analytic expression for the carrier DF considers both low and high energy carriers. The problem is that the DFs in nLDMOS devices have a different shape compared to those simulated for planar nMOSFETs [1,3]. The DD scheme was suggested to be applicable for the devices with gate lengths longer that 0.5µm. However, as we showed in [4], the drift-diffusion and hydrodynamic approaches can be inadequate for HCD modeling even in nMOSFETs with gate lengths of 2.0µm**.** In this context, the analysis of the limits of the model validity is an important task. For this purpose, we use a series of nMOSFETs of a similar architecture but with different gate lengths.

2. The Modeling Framework

Our HCD model covers and links carrier transport, the microscopic mechanisms of Si-H bond dissociation, and simulation of the degraded devices. There are two different versions of the model used: the first is based on the exact BTE solution with the SHE method, while the second one uses the analytic DD-based expression for the carrier DF [1,3]. The device architecture is obtained using the Sentaurus process simulator which was coupled with our DD-based process simulator MiniMOS-NT. For device simulations we use a highly adaptive meshing framework ViennaMesh which generates meshes using the built-in potential. As for the defect generation level, we consider all the superpositions of single- and multiple-carrier processes of bond rupture and the stochastic variations of the bond-breakage activation energy as well as its reduction due to the dipole-field interactions [1]. The interface state profiles calculated with this model are then used in our device simulator MiniMOS-NT to evaluate the degradation characteristics of the damaged device.

The both versions of the model are capable of representing HCD in nLDMOS devices stressed at different combinations of drain (V_{ds}) and gate voltages (V_{gs}). Fig. 1 shows the electron DFs simulated for V_{ds} = 18V and V_{gs} = 2V for different device sections using the SHE method and the DD-based model. The experimental change of the linear drain current ($\Delta I_{d,lin}$) is plotted vs. stress time in Fig. 2 and is represented by both versions of the model with good accuracy. From Figs. 1,2 one concludes that the results of SHE- and DD-based models are almost identical. In order to analyze whether the DD-based model can capture HCD in nMOSFETs we used the Sentaurus process simulator and simulated three nMOSFETs of a similar topology but with three gate lengths (L_G) of 2.0, 1.5, and 1.0µm.

3. Results and Discussions

The electron DFs, interface state density profiles $N_{it}(x)$, and the degradation traces $\Delta I_{d,lin}(t)$ were simulated for V_{ds} = 7.5V and V_{gs} = 2.5V with SHE- and DD-based versions of the model, Figs. 3-11. Note that stressed voltages used are more typical for these nMOSFETs (e.g. [4,5]) and are lower than those applied in the case of the nLDMOS devices. From Figs. 3,6,9 one can see that at low and moderate energies the DFs obtained from ViennaSHE can be reasonably mimicked by the analytic model. At higher energies, the curvature of DFs computed with the two approaches is different. At these energies, the occupation numbers, however, have dropped by several orders of magnitude, and it is not obvious whether this discrepancy in DFs translates into error in N_{it} and $\Delta I_{d,lin}$ values. Figs. 4,7,10 suggest that in the case of the longest device $N_{it}(x)$ profiles are very similar, while for shorter counterparts agreement deteriorates. For L_G = 1.5µm the discrepancy between N_{it} values is visible at the level of ~10^8cm^{-2}, while if L_G = 1.0µm the densities differ already at the 10^{12}cm^{-2} level. As a result, best correspondence between SHE- and DD-based $\Delta I_{d,lin}(t)$ traces is achieved for the 2.0µm nMOSFET and this correspondence aggravates when the device dimensions shrink. Note that even for L_G = 2µm the analytic model leads to lower $\Delta I_{d,lin}$ values at short stress times. This is because, as we showed in [3], short-term HCD is determined by the drain DFs underestimated by the analytic model (see Fig. 3).

4. Conclusions

We have found out that the analytic HCD model works reasonably well in terms of the DFs, $N_{it}(x)$ profiles, and $\Delta I_{d,lin}(t)$ degradation traces for the 2.0µm nMOSFET. The situation starts to change for the 1.5µm device. The reason is that the analytic model is not able to catch the more complicated DF shape. For L_G = 1.5µm the DD-based model results are still reasonable, while for L_G = 1.0µm the analytic model completely fails to predict HCD.

References

[1] M.Bina *et al.*, IEEE TED 61, p. 3103 (2014). [2] Y.M. Randriamihaja *et al.*, Microel. Reliab. 52, p. 2513 (2012). [3] P. Sharma *et al.*, IEEE TED 62, p. 1 (2015). [4] S. Tyaginov *et al.*, ESS-DERC-2011, p. 151. [5] S. Tyaginov *et al.*, SISPAD 2011, p. 123 [6] A. Bravaix *et al.*, ESREF-2010, tutorial.

Acknowledgements

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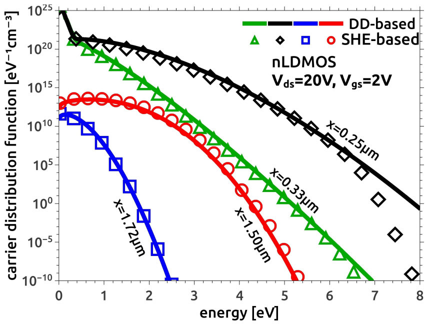

Fig. 1. The DFs at different values of the lateral coordinate for the nLDMOS device.

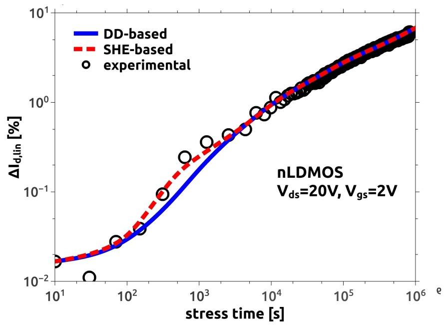

Fig. 2. $\Delta I_{\mathrm{d,lin}}$ degradation: experiment vs. simulation using the SHE- and DD-based model.

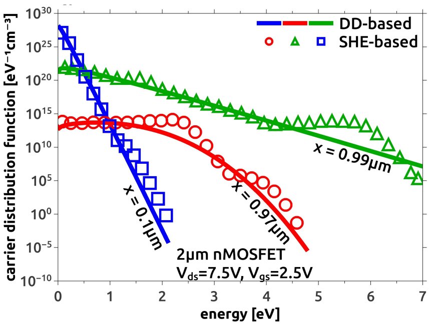

Fig. 3. The DFs at different lateral coordinate for the 2.0µm device.

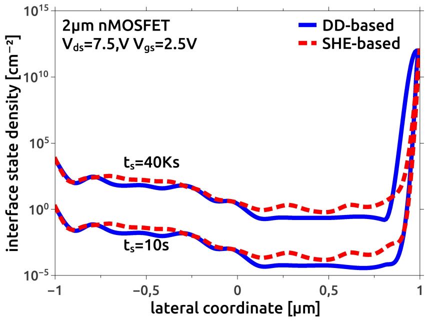

Fig. 4. The $N_{\mathrm{it}}(x)$ profiles evaluated for the 2.0µm device with both versions of the model for stress times of 10s and 40ks.

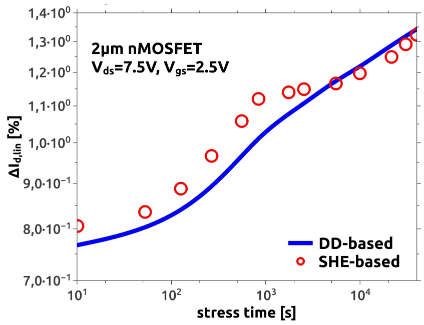

Fig. 5. The $\Delta I_{\mathrm{d,lin}}$ degradation curves obtained for the 2.0µm device with both versions of the model. Reasonable agreement between the versions is achieved.

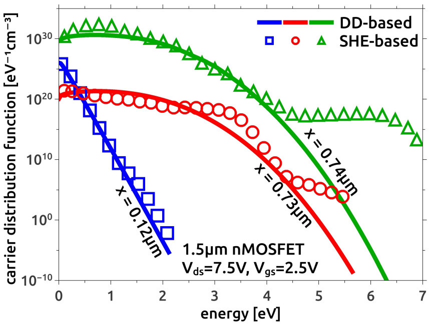

Fig. 6. The DFs at different lateral coordinate for the 1.5µm device.

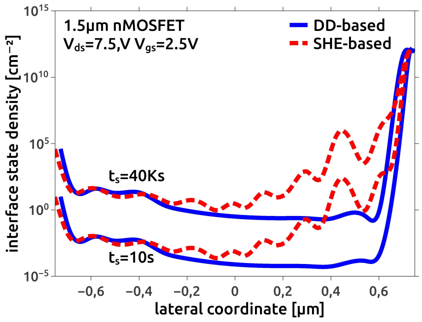

Fig. 7. The $N_{\mathrm{it}}(x)$ profiles evaluated for the 1.5µm device with both versions of the model for stress times of 10s and 40ks.

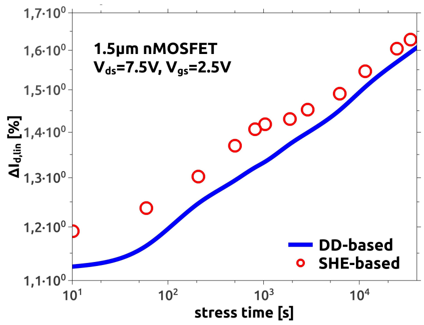

Fig. 8. The $\Delta I_{\mathrm{d,lin}}$ degradation curves obtained for the 1.5µm device with both versions of the model.

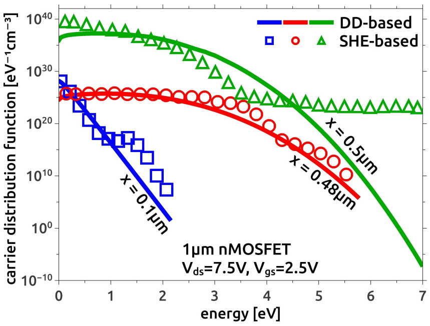

Fig. 9. The DFs at different lateral coordinate for the 1.0µm device.

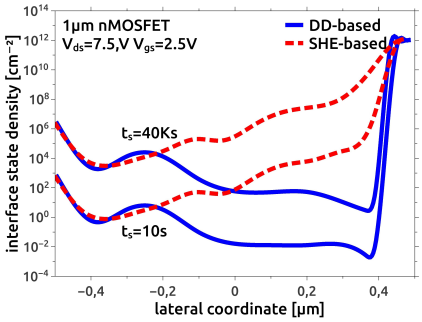

Fig. 10. The $N_{\mathrm{it}}(x)$ profiles evaluated for the 1.0µm device with both versions of the model for stress times of 10s and 40ks.

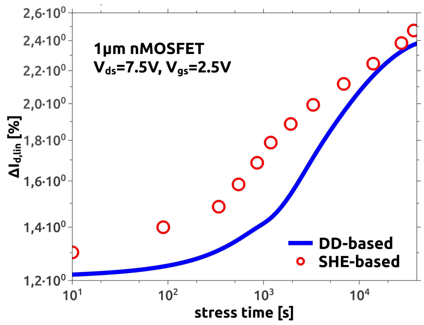

Fig. 11. The $\Delta I_{\mathrm{d,lin}}$ degradation curves obtained for the 1.0µm device with both versions of the model. The DD model fails to predict HCD.