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Investigation of Backgating Effect on Superlinear Onset of Output Characteristics for UTB III-V Heterojunction Tunnel FET

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Abstract

This work investigates the backgating effect on the superlinear onset of output characteristics for III-V ultra-thin-body broken-gap heterojunction tunnel FET (HTFET). Our study indicates that applying reverse backgate bias not only reduces the OFF-state leakage, but also improves the superlinear onset behavior which is crucial to TFET logic circuits. We also show that the conflict between the transfer characteristic and the output characteristic of p-type HTFET regarding the source doping can be mitigated by backgating.

Introduction

Tunnel FET (TFET) [1] is a promising post-CMOS device candidate for low supply-voltage operation. To surmount the problem of low ON-current (I_{on}) for Si TFET, III-V TFET with direct band-gap and smaller effective mass has been proposed [2]. With a broken-gap offset near the source/channel junction, the GaSb/InAs (6.1-Å lattice family) heterojunction TFET (HTFET) shows ultra-thin tunneling barrier resulting in high I_{on} and becomes one of the leading options for future low-power applications.

However, the drawback of superlinear onset of output characteristics (delayed current saturation) typical of TFET devices [3]-[5] remains and affects the performance of HTFET. In this work, we investigate this critical problem and show the impact of backgate biasing on the superlinear onset behavior for ultra-thin-body (UTB) HTFET.

Methodology

Table I shows the pertinent materials and dimensions of the p-type HTFET (pHTFET) in this study. We use the non-local band-to-band tunneling (BTBT) model [6] to account for the arbitrary tunneling barrier with non-uniform electrical field. The non-local BTBT model parameters (Table II) have been calibrated [2][7].

Results and Discussion

Figures 1 and 2 illustrate the conflict between the transfer characteristic and the superlinear onset of output characteristics regarding the source doping (N_{SOURCE}). Due to the low conduction-band density-of-states (DOS) in InAs source (n region) leading to the Fermi-tail limited tunneling current [Fig. 1(a)], the pHTFET with N_{SOURCE} = 1E18 cm^{-3} possesses a superior transfer characteristic than that of N_{SOURCE} = 4E19 cm^{-3} [Fig. 1(b)]. However, the superlinear onset of output characteristics degrades with decreasing N_{SOURCE} as shown in Fig. 2.

To explain Fig. 2, Fig. 3 shows the energy band diagram at the HK/channel interface of the pHTFET under varying drain bias (V_{SD}). It can be seen that the energy band of source side with N_{SOURCE} = 4E19 cm^{-3} does not vary with V_{SD} and keeps the ultrathin tunneling barrier. However, the source-side energy band with N_{SOURCE} = 1E18 cm^{-3} is altered by increasing V_{SD}, resulting in the degraded superlinear onset behavior (Fig. 2).

To overcome the conflict between the transfer characteristic and the superlinear onset of output characteristics, we investigate the impact of backgate bias (V_{SB}) on the pHTFET with N_{SOURCE} = 1E18 cm^{-3}. Fig. 4 shows the impact of V_{SB} on the transfer characteristic. It can be seen that with a reverse V_{SB} ($V_{SB} < 0$), the OFF-current can be significantly reduced [7]. The output characteristics for the pHTFET with various V_{SB} are shown in Fig. 5. An improvement in the superlinear onset behavior with reverse backgate biasing can be clearly seen. Fig. 6 further confirms the impact of V_{SB} on the superlinear onset behavior using output conductance (g_{ds}) [Fig.6 (a)] and the derivative of g_{ds} [Fig. 6(b)].

The beneficial effect of reverse backgate biasing on the superlinear onset behavior can be explained by the band diagrams shown in Fig. 7.

We also examine the backgating effect on the HTFET based inverter. Fig. 8 shows the transient responses of the inverter with varying backgating bias V_B on the pHTFET (with V_S = V_{DD}). It can be seen that the rise-time delay (output low-to-high) significantly improves with increasing V_B, thus showing the importance of addressing the superlinear onset behavior for TFET logic circuits.

It should be noted that albeit in this work we use p-type HTFET to demonstrate the backgating effect on the superlinear onset of output characteristics, similar effect exists for n-type HTFET.

Acknowledgement

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References

[1] A. M. Ionescu *et al.*, *Nature*, vol. 479, no. 7373, p. 329, 2011.
[2] M. Luisier *et al.*, *IEDM Tech. Dig.*, p. 913, Dec. 2009.
[3] E. Gnani *et al.*, *Proc. ESSDERC*, p. 105, Sep. 2012.
[4] A. Pal *et al.*, *IEEE TED*, vol. 58, no. 4, p. 1045, Mar. 2011.
[5] L. D. Michielis *et al.*, *IEEE EDL*, vol. 33, no. 11, p. 1523, Nov. 2012.
[6] *Sentaurus* TCAD, Synopsys, Inc., Mountain View, USA, 2011.
[7] M.-L. Fan *et al.*, *IEEE TED*, vol. 62, no. 1, p. 107, Jan. 2015.

Table I. The materials for source, channel and drain of the UTB structure and relevant device dimensions. The drain is lightly doped to mitigate the ambipolar effect.

Device	Source (n)	Channel (i)	Drain (p)
P-type HTFET	InAs	GaSb	

L_g	T_{ch}	EOT	T_{BOX}
25 nm	5 nm	0.65 nm	10 nm

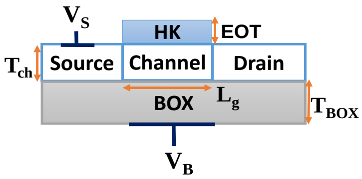

Table II. Pertinent model paprameters for nonlocal BTBT.

Parameter	InAs	GaSb
Bandgap, E_g (eV)	0.504	0.864
Electron Affinity (eV)	4.9	4.06
Tunneling parameter, A_{Path}	3×10^{19}	2.7×10^{20}
Tunneling parameter, B_{Path}	2.6×10^{6}	1.2×10^{7}
Tunneling parameter, R_{Path}	1.13	1.12
Conduction Band DOS, N_C (cm^{-3})	8.72×10^{16}	2.1×10^{17}
Valence Band DOS, N_V (cm^{-3})	6.66×10^{18}	1.8×10^{19}

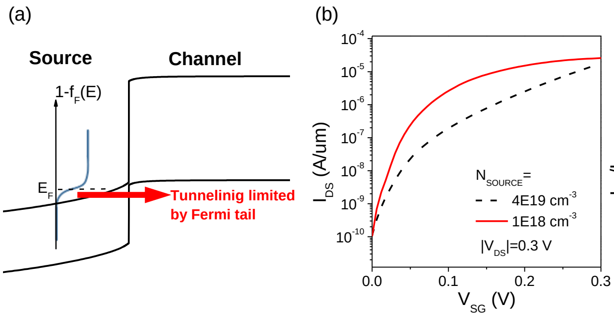

Fig. 1. (a) Band diagram of source/channel junction showing the cause of transfer characteristics degradation for pHTFET with high N_{SOURCE}. (b) I_{DS}-V_{SG} transfer-characteristics comparison for pHTFET with varies N_{SOURCE}.

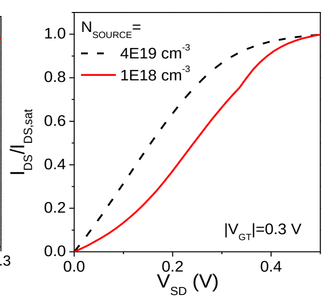

Fig. 2. Impact of N_{SOURCE} on the output characteristics at V_{DD}= 0.3 V, and normalize with their saturation current $I_{DS,sat}$.

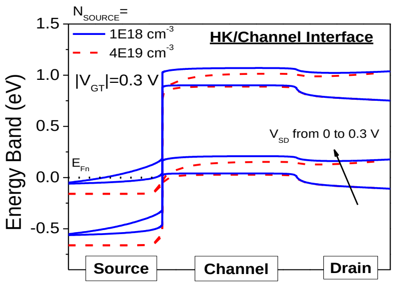

Fig. 3. Energy band diagram for pHTFET with different N_{SOURCE} across HK/Channel interface.

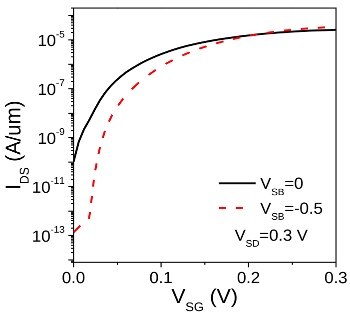

Fig. 4. Impact of V_{SB} on the I_{DS} -V_{SG} characteristics of pHTFET.

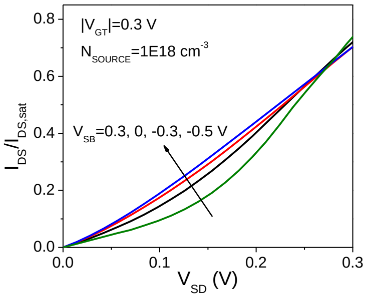

Fig. 5. Impact of V_{SB} on the output characteristics of pHTFET.

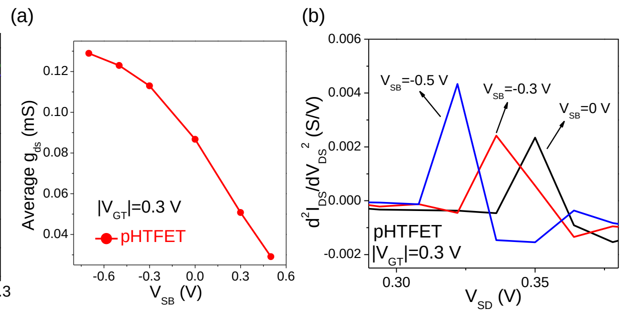

Fig. 6. (a) Average output conductance (g_{DS}) at low V_{SD} (below 0.25V), and (b) Derivative of the output conductance of pHTFET for varies V_{SB}.

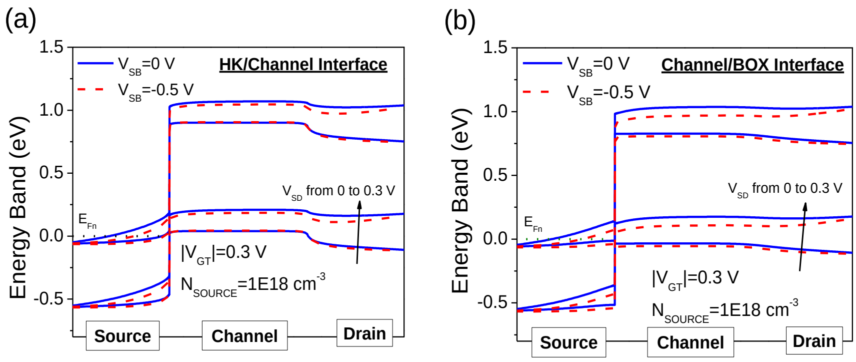

Fig. 7. Impact of V_{SB} on the energy band diagram of pHTFET across (a) HK/Channel interface, and (b) Channel/BOX interface in the superlinear region (V_{SD} from 0 to 0.3 V).

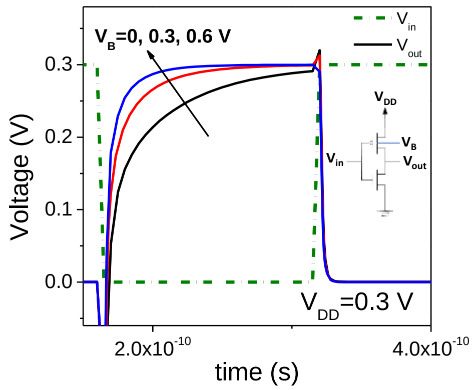

Fig. 8. Transient response of HTFET-based inverter considering the impact of reverse backgate bias V_B on pHTFET.