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Optimized Nanowire Diameter for III-V Homojunction and Heterojunction Gate-All-Around Tunnel FETs

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Abstract- This work explores the optimized nanowire diameter for III-V homojunction and heterojunction gate-all-around tunnel FETs (TFETs). Our study indicates that, in spite of excellent gate control, there is no gain in I_{60mV} and I_{on}/I_{off} with too small a diameter for the III-V TFETs because of the quantum-confinement increased tunneling width. For the broken-gap heterojunction TFET (HTFET), the optimized diameter occurs before the band alignment changes. In addition, the optimized diameter for the I_{on}/I_{off} decreases with decreasing channel length for the InAs TFET because of its worse drain induced barrier thinning (DIBT) than the HTFET.

Introduction

Tunnel FET (TFET) is a promising post-CMOS device candidate that may possess a subthreshod swing smaller than the (2.3)kT/q limit of MOSFET [1]. Since Si TFETs usually possess low ON currents (I_{on}), III-V TFETs with small/direct bandgap and high I_{on} are especially important [4]. In addition, TFETs with gate-all-around (GAA) nanowire structures are also attractive because the superior gate control enabled by the GAA structure is crucial to the gate induced band-to-band tunneling (BTBT) mechanism.

Although the gate control increases with decreasing nanowire diameter, the effective bandgap of III-V TFETs also increases (which degrades the BTBT) with decreasing nanowire diameter due to quantum confinement [2]. Whether there is an optimized diameter design for nanowire III-V TFETs is an important question and merits investigation. In this work, we tackle the problem by examining the homojunction InAs TFET and the heterojunction broken-gap TFET (HTFET) [4] using TCAD simulations.

Methodology

Fig. 1 shows a schematic sketch of the GAA structure in this study. For the HTFET, we consider the GaSb/InAs (6.1-Å lattice family) with a broken-gap offset near the source/channel junction that enables ultra-thin tunneling barrier and high I_{on} [4]. We employ the dynamic nonlocal BTBT model during TCAD simulation [3]. As shown in Fig. 2, we calibrate our BTBT model with the fully-band atomistic quantum transport results [4][5]. In addition, we calculate the effective bandgap widening with considering the wavefunction penetration into the high-K dielectric (HfO_2) [6]. We correct the band profile (affinity and bandgap) and the BTBT model parameters (A and B) according to Eqns. (1)-(4) in Fig. 2.

We use I_{60mV} and I_{on}/I_{off} as the targets of our diameter optimization. The I_{60mV} is defined as the drain current (per cross-sectional area) at which the subthreshold swing is equal to 60 mV/decade.

Results and Discussion

Fig. 3 (a) and (b) show the diameter dependence of the I_{60mV} and I_{on}/I_{off}, respectively, for InAs TFETs with varying equivalent oxide thickness (EOT). It can be seen that the diameter dependences are non-monotonic. For both the I_{60mV} and I_{on}/I_{off}, there exists a diameter range where the TFET performances are the best. This is due to the counterbalance between the gate control and quantum confinement. In other words, in spite of excellent gate control, there is no gain in I_{60mV} and I_{on}/I_{off} with too small a diameter because of the quantum-confinement increased tunneling width. It is also noted from Fig. 3 that when designed with the optimized diameter, the TFET performance variation due to diameter variation can also be suppressed because it is where the minimum diameter sensitivity occurs.

Fig. 4 (a) and (b) also show non-monotonic diameter dependences of the I_{60mV} and I_{on}/I_{off} for HTFETs, albeit the diameter range for optimized I_{60mV} and I_{on}/I_{off} becomes narrower than that of the InAs TFET. Since the HTFET possesses an ultra-thin tunneling barrier, it can maintain very small tunneling width with decreasing diameter until its band alignment changes from type-III to type-II as shown in Fig. 4(c).

To investigate the impact of gate length (L_g) on the optimized diameter, Fig. 5 (a) and (b) show the diameter dependences of the I_{60mV} and I_{on}/I_{off} for InAs TFETs with varying L_g. It can be seen that both the I_{60mV} and I_{on}/I_{off} decrease with decreasing L_g due to drain induced barrier thinning (DIBT) [7]. Moreover, the optimized diameter for I_{on}/I_{off} decreases with decreasing L_g (e.g., L_g = 10nm).

For HTFETs, however, the optimized diameter for both the I_{60mV} and I_{on}/I_{off} does not change with L_g as shown in Fig. 6. This is because the HTFET possesses superior immunity to DIBT than the InAs TFET as shown in Fig. 7. Fig. 8 shows that the tunneling width is more sensitive to varying drain voltage for the InAs TFET as compared with the HTFET.

Acknowledgement

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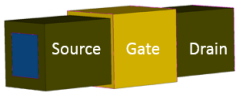

Device	Source(p)	Channel(i)	Drain(n)
Homojunction TFET	InAs		
Heterojunction TFET	GaSb	InAs	

Fig. 1. Schematic sketch of a GAA structure. The source doping is 4×10^{19} cm^{-3}, while the drain doping is 6×10^{17} cm^{-3} to suppress the ambipolar behavior. The supply voltage is 0.3V.

Calibrate BTBT model parameters for the heterojunction [4] and homojunction [5] TFETs

$$R_{net} = A\left(\frac{F}{F_0}\right)^P \exp\left(\frac{-B}{F}\right) \quad (1)$$

Calculate the effective bandgap widening [6]

$$A = \frac{g\pi m_r^{1/2}(qF_0)^2}{9h^2E_g^{1/2}} \quad (2)$$

Change the band profile (bandgap and affinity) and BTBT model parameters (A and B)

$$B = \frac{\pi^2 m_r^{1/2} E_g^{3/2}}{qh} \quad (3)$$

TCAD Simulation

$$\frac{1}{m_r} = \frac{1}{m_c} + \frac{1}{m_v} \quad (4)$$

Fig. 2. Methodology used in this work. R_{net} is the BTBT generation rate and P=2. F is the electric field and F_0=1V/cm. g is the degeneracy factor and E_g is the bandgap. m_v and m_c are the effective mass of conduction band and valence band.

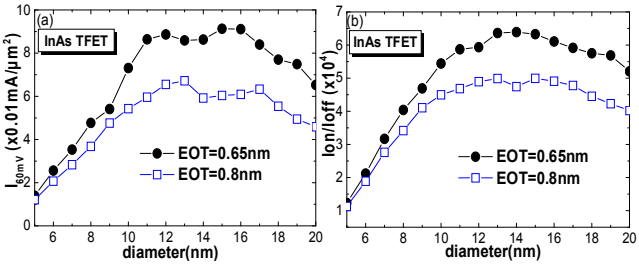

Fig. 3. I_{60mV} and I_{on}/I_{off} versus diameter for InAs TFET with various EOT and Lg=20nm.

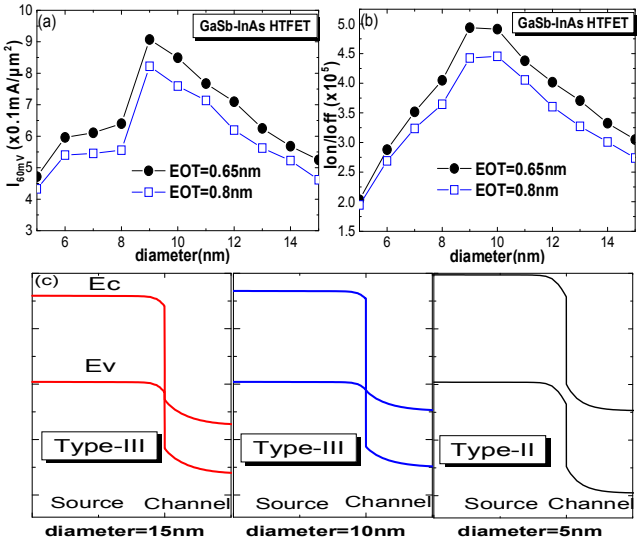

Fig. 4. (a)(b) I_{60mV} and I_{on}/I_{off} versus diameter for GaSb-InAs HTFET with various EOT and Lg=20nm. (c) The band alignment changes from type-III to type-II with decreasing diameter.

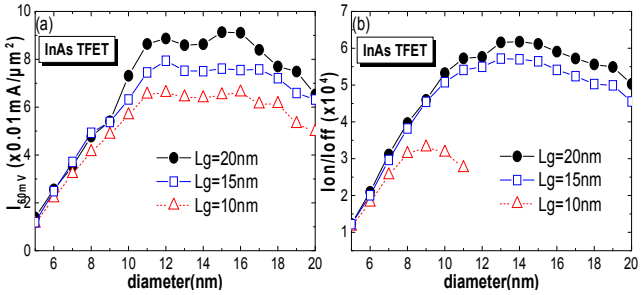

Fig. 5. I_{60mV} and I_{on}/I_{off} versus diameter for InAs TFET with various Lg and EOT=0.65nm.

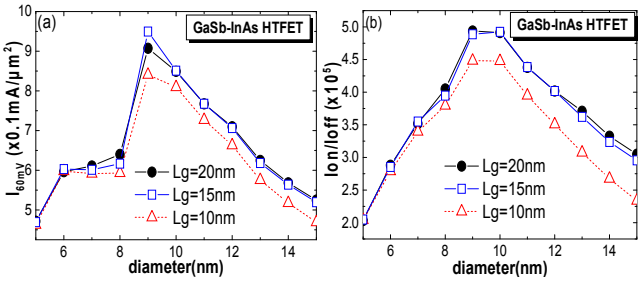

Fig. 6. I_{60mV} and I_{on}/I_{off} versus diameter for GaSb-InAs HTFET with various Lg and EOT=0.65nm.

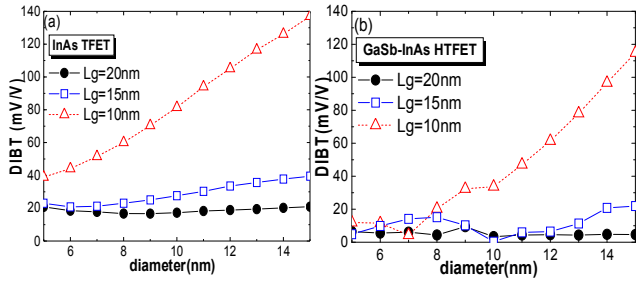

Fig. 7. DIBT versus diameter for InAs TFET and GaSb-InAs HTFET. DIBT is defined as the Vt reduction (constant current=10^{-1}mA/μm^2 [7]) as V_{DS} increases from 30mV to 0.3V.

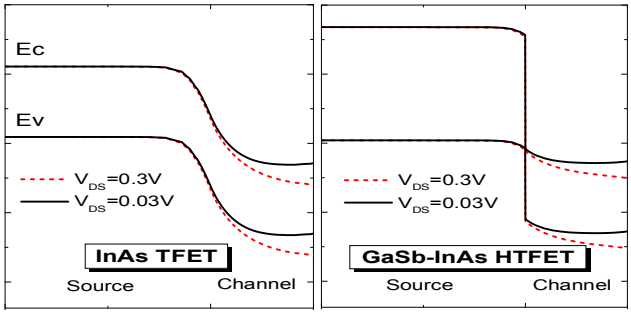

Fig. 8. Band diagram of the source-channel junction for InAs TFET and GaSb-InAs HTFET with V_{DS}=0.3V and V_{DS}=0.03V when the diameter=10nm and the gate length=10nm.