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Transmission Line Model and Transconductance Method for Layout Dependent Source Resistance Extraction in Multi-Finger MOSFETs

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Abstract

A new method based on transmission line (TML) model is developed for an accurate extraction of the source resistance (R_S) in multi-finger (MF) MOSFETs with different poly-to-poly (PO-PO) spaces and source line routing. The R_S determined by TML model can consistently predict the degradation of normalized transconductance (g_m) in MF devices compared to single-finger (SF) devices with negligibly small R_S. The wide PO-PO space used in MF devices intends to increase the tensile stress from contact etching stop layer (CESL) and yield higher electron mobility but leads to the penalty of larger R_S. The adoption of two-end source line can achieve more than 60% R_S reduction and eliminate the penalty caused by wide PO-PO space. This new method can realize an efficient and precise extraction of R_S in various layouts and facilitate MF devices layout optimization as well as simulation accuracy for high performance design.

I. Introduction

Multi-finger (MF) layout has been widely used in RF and analog circuits for gate resistance (R_g) reduction to achieve higher f_{MAX} and lower noise **[1]-[3].** Unfortunately, the increase of finger number (N_F) and reduction of finger width (W_F) for smaller R_g lead to larger R_S due to longer source line and lower effective mobility (μ_{eff}) due to stronger STI transverse tress ($\sigma_\perp$). Both of which result in g_m degradation and further impact on f_T, f_{MAX}, and RF noise. The wide PO-PO space is considered a solution in MF devices to increase CESL induced tensile stress and yield higher nMOS μ_{eff}, which can relieve the g_m degradation **[4]**. However, the potential increase of R_S due to extended source line caused by wide PO-PO space may offset the benefit from tensile stress. Two-end source line is proposed to reduce R_S and recover the performance. Unfortunately, the short deembedding method used in high frequency characterization cannot extract the R_S experienced by MF devices incorporating distributed metal line, stacked vias, and contacts on source/drain. For the first time, a new method for R_S extraction, namely transmission line (TML) model, has been developed in this paper. An extensive benchmark will be performed on various methods, such as short deembedding method, g_m method, and our TML model to identify the best solution in terms of accuracy, efficiency, and cost.

II. Layout Dependence of g_m in MF and SF Devices

MF and SF nMOSFETs with the same splits of W_F (2, 0.5, and 0.25μm) were fabricated in 90nm RF CMOS process. Fig.1(a)~(c) illustrate the MF layouts with simultaneously varied W_F and N_F , namely W2N16, W05N64, and W025N128, with fixed total width, $W_{tot}=W_F \times N_F$ =32 μm. Herein, $\sigma_{//}$ and $\sigma_\perp$ denote the longitudinal and transverse stresses introduced from STI. Standard and wide PO-PO spaces with S_{PO-PO}=0.28 μm and 0.44 μm, were designed to vary the tensile $\sigma_{//}$ from CESL and verify the influence on μ_{eff} and g_m. Two-end source line denoted as "2S" was adopted in W025N128.2S with standard PO-PO space, and W05N64wsd.2S as well as W025N128wsd.2S with wide PO-PO space, trying to reduce R_S. **Fig. 2**(a)~(c) presents a comparison of the normalized g_m, i.e. g_m/W_{tot} vs. V_{GT} between the SF and MF devices with the same W_F. The results reveal an apparent degradation of g_m/W_{tot} in W05N64 and W025N128 compared to W05N1 and W025N1 (Fig.2(b) and (c)). W025N128.2S adopting two-end source line can improve $g_{m,max}/W_{tot}$ by 8.3% w.r.t. W025N128, but still suffer 11.6% degradation compared to W025N1. The differences between the SF and MF devices indicates that R_S is a key parameter responsible for g_m/W_{tot} degradation.

III. TML Model and g_m Method for R_S Extraction

In the following, a new method, namely TML model is developed for an accurate extraction of R_S in MF devices. **Fig. 3**(a) and (b) illustrate the cross sectional view of MF devices with single- and two-end source line routing. Taking these two structures and current flow through the source line, TML model can be represented by **Fig. 4** (a) and (b) for single- and two-end source lines, respectively. Thus, R_S can be calculated according to (1)~(10) for single-end source line, and (11)~(13) for two-end source line.

$$V_1 = I_{dsat} \cdot R_{M3,end} \quad (1) \quad V_{s,1} = V_1 + I_s \cdot R_{CT,via} \quad (2) \quad R_{s,1} = V_{s,1} / I_s \quad (3)$$

$$V_i = V_{i-1} + I_{i-1} \cdot R_{M3} \quad (4) \quad V_{s,i} = V_i + I_s \cdot R_{CT,via} \quad (5) \quad R_{s,i} = V_{s,i} / I_s \quad (6)$$

$$I_{dsat} / \left(N_F / 2 + 1\right) \quad (7) \quad \Delta R_{s,i-1} = \left(V_{s,(N_F/2+1)} - V_{s,i-1}\right) / I_s \quad (8)$$

$$R_{s,i-1}' = R_{s,i-1} + \Delta R_{s,i-1} = V_{s,(N_F/2+1)} / I_s = R_{s,(N_F/2+1)} \quad (9)$$

$$R_{s(single-end)} = R_{s,1}' \| R_{s,2}' \| \ldots \| R_{s,(N_F/2+1)}' \quad (10) \quad i = 2,\ 3..N_F/2+1$$

$$R_{s,i-1}' = V_{s,(N_F/4+1)} / I_s = R_{s,(N_F/4+1)},\ \ i = 2,\ 3.....N_F/4+1 \quad (11)$$

$$R_{s,j+1}' = V_{s,(N_F/4+1)} / I_s = R_{s,(N_F/4+1)},\ \ j = N_F/4+1,\ .....,N_F/2 \quad (12)$$

$$R_{s(two-end)} = R_{s,1}' \| .. \| R_{s,(N_F/4+1)}' \| .. \| R_{s,(N_F/2+1)}' \quad (13)$$

Fig. 5 presents R_S vs. N_F determined by this TML model for MF devices with different PO-PO spaces and source line routing. The results for standard MF devices with single-end source line demonstrate a perfect linear function and more than 6 times increase of R_S from 0.77Ω for W2N16 to 5.427 Ω for W025N128. As for W025N128.2S using two-end source line, the R_S can be reduced to as small as 1.87Ω, which is around 66% reduction compared to W025N128. A comparison of W2N26 and W2N16wsd, both using single-end source line, indicates around 14.3% higher R_S in W2N16wsd with wide PO-PO space due to longer source line. Encouragingly, the adoption of two-end source line in wide PO-PO space can realize more than 50% R_S reduction compared to the standard PO-PO space with single-end source line, and reverse the layout dependence, such that W05N64wsd.2S < W025N128wsd.2S < W05N64.

In case that SF devices with negligible R_S are available on the same chip to serve as an ideal reference, R_S can be extracted by g_m method based on the g_m difference between MF and SF devices with the same W_F, according to (14)~(16). Note that g_{m0} represents the ideal g_m free from R_S, equal to $g_{m(SF)}$ measured from SF devices and multiplied by N_F, given by (16).

$$g_m = g_{m0} / \left(1 + g_{m0} R_S\right) (14) \quad R_S = 1/g_m - 1/g_{m0} (15) \quad g_{m0} = g_{m(SF)} \cdot N_F (16)$$

As shown in **Fig. 6**, R_S vs. N_F achieved by the g_m method indicates a good consistency with those predicted by TML model (Fg.5). Again, the standard PO-PO space with single-end source line approaches a perfect linear curve. The wide PO-PO space with two-end source line can yield more 50% smaller R_S than the

standard one with single-end source line and lead to a curve far below the standard MF layouts. This good agreement between g_m method and TML model can validate our new method in terms of accuracy and advantages such as efficiency and lower cost, due to saving extra chip area and measurement for SF devices.

Moreover, short deembedding method was performed, taking S-parameters measured from short- and open-deembedding structures, and extraction flow given by (17)~(20) to extract R_S. As shown in **Fig.7**, the R_S vs. N_F behaves a perfect linear function but reveals abnormally small value compared with those achieved by using g_m method and TML model. The results suggest that short deembedding method cannot extract the actual R_S experienced by MF devices incorporating distributed metal line, stacked vias, and contacts on source/drain. Besides, short deembedding cannot identify the difference in source line layout and gives nearly the same R_S for single- and two-end source line routing.

$$S_{open} \rightarrow Y_{open}\ ;\ S_{short} \rightarrow Y_{short} \quad (17) \qquad Y_{short\_o} = Y_{open} - Y_{short} \quad (18)$$

$$Y_{short\_o} \rightarrow Z_{short\_o} \quad (19) \qquad R_S = Re\left(Z_{12}^{short\_o}\right) \quad (20)$$

IV. Conclusion

Our developed TML model can realize an accurate extraction of R_S in MF devices, without resort to SF devices required for g_m method. The adoption of two-end source line in wide PO-PO space can yield more than 50% R_S reduction compared to the standard PO-PO space with single-end source line. This method can facilitate MF layout optimization for g_m enhancement, due to higher mobility and lower R_S.

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References

[1] L.F. Tiemeijer *et al.*, *IEDM Tech. Dig.*, pp.441-444, 2004.
[2] I. Post *et al.*, *IEDM Tech. Dig.*, ,pp.1013-1015, 2006.
[3] H. Li *et al.*, *VLSI Tech. Symp. Proc.*, pp.56-57, 2007.
[4] A. Oishi *et al.*, *IEDM Tech. Dig.*, ,pp. 229-232, 2005.

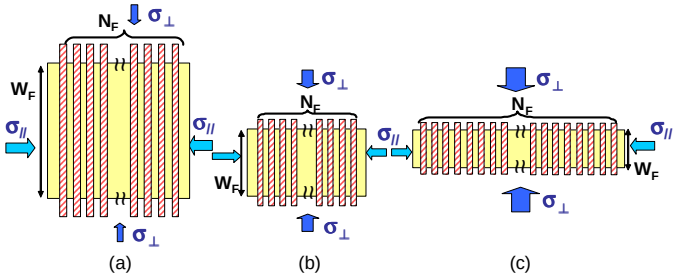

Fig. 1. Schematics of multi-finger MOSFETs with fixed $W_F \times N_F$ =32μm (a) W2N16 : $W_F \times N_F$ =2μm×16 (b) W05N64 : $W_F \times N_F$ =0.5μm×64, (c) W025N128 : $W_F \times N_F$ =0.25μm×128.

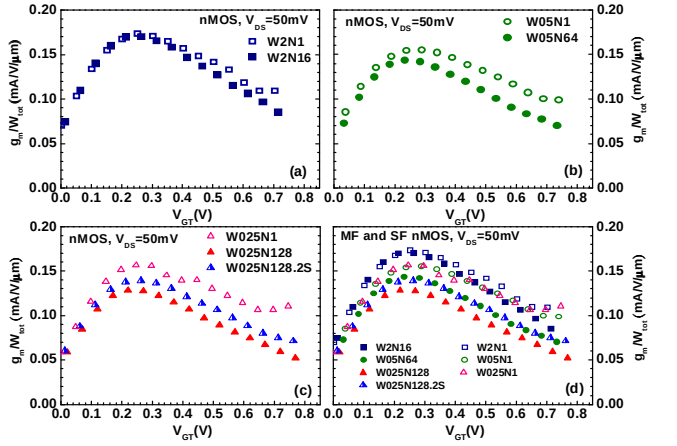

Fig.2 Comparison of g_m/W_{tot} vs. V_{GT} (V_{DS}=50mV) measured from single-finger and multi-finger nMOSFETs (a) W2N1 and W2N16 (b) W05N1 and W05N64 (c) W025N1, W025N128, W025N128.2S (d) all single- and multi-finger devices. 2S : two-end source line.

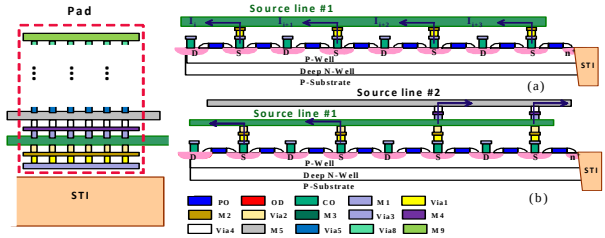

Fig.3 Schematics of MF devices with (a) single-end source line (b) two-end source lines.

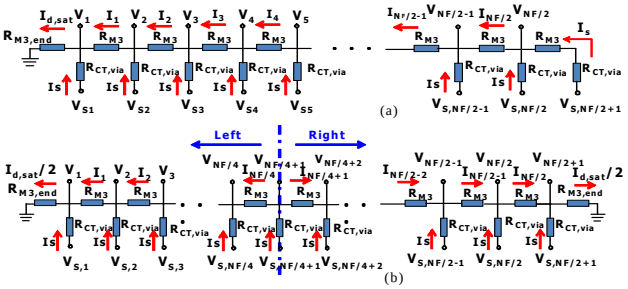

Fig.4 TML model for calculating R_S in MF devices with (a) single-end source line (b) two-end source lines.

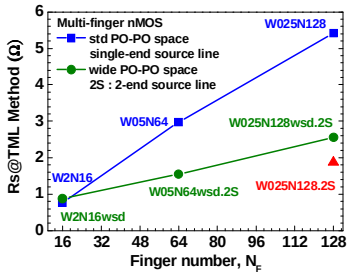

Fig. 5 R_S vs. N_F determined by TML method for MF nMOS with standard PO-PO space : W2N16, W05N64, W025N128, and W025N128.2S, and wide PO-PO space : W2N16wsd, W05N64wsd.2S, and W025N128wsd.2S. 2S : two-end source line.

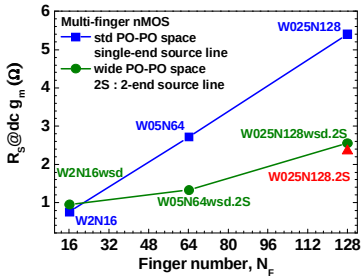

Fig.6 R_S vs. N_F determined by g_m method applied SF and MF nMOS with the same W_F. MF nMOS with standard PO-PO space : W2N16, W05N64, W025N128, W025N128.2S. nMOS with wide PO-PO space : W2N16wsd, W05N64wsd.2S, and W025N128wsd.2S. 2S : two-end source line.

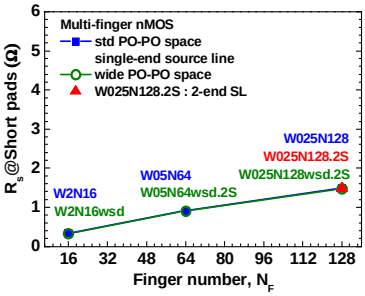

Fig.7. R_S vs. N_F extracted from short deembedding structures for MF nMOS. Standard PO-PO space : W2N16, W05N64, W025N128, and W025N128.2S. Wide PO-PO space : W2N16wsd, W05N64wsd.2S, and W025N128wsd.2S. 2S : two-end source line.