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Comparative Study of Tunnel Field Effect Transistors with Dopant-Segregated Schottky Source/Drain

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Abstract

Dopant-segregated Schottky source/drain (S/D) tunnel field effect transistors (STFET) are investigated. The working mechanisms of STFET and the influence of device parameters are studied with Synopsys Sentaurus. STFET has similar performance as TFET in spite of the existence of Schottky contact. High segregation doping for STFET is required to increase tunneling probability and suppress bipolar behaviors. Increasing *eSBH* at source side helps to reduce hole barrier and improve drive current. Furthermore, STFET is also insensitive to segregation length and the barrier at drain side, which would relax the requirement for S/D fabrication.

1. Introduction

Tunnel field effect transistors (TFET) has raised much attention these days, because of steep subthreshold slope (*SS*) and low Off-state current.[1-3] However, TFET suffers from problems such as large junction steepness and trap assisted tunneling (TAT) caused by ion implantation and thermal annealing.[3] Recently, dopant-segregated Schottky barrier tunnel field effect transistors (STFET) has been proposed to overcome these difficulties.[4] Schottky S/D replaces conventional junctions with metal silicide, and dopant segregation (DS) is formed by ion implantation into silicide at tilted angles of 45° and 135° using the gate stack as a shadow mask.[4] Nevertheless, Schottky barrier at S/D could reduce drive current and have effect on other characteristics. In this paper, we focus on double-gate silicon STFET to investigate its transport behaviors and electrical properties. The influence of physical parameters has also been discussed by comparing with TFET.

2. Device structure and simulation parameters

The schematic structures and energy band diagrams of TFET and STFET are shown in Figs. 1(a) and 1(b), respectively. For both TFET and STFET, the gate length, L_g = 16 nm, and the equivalent gate oxide thickness, T_{ox} = 1 nm. The default silicon thickness, T_{si} = 10 nm, and the channel doping, N_{ch} = 10^{15} cm^{-3}. For TFET, a p-type source and an n-type drain are used in the simulation. The default source/drain (S/D) length, $L_{s/d}$ = 20 nm, and the S/D doping, $N_{s/d}$ = 10^{20} cm^{-3}. For STFET, S/D contacts are replaced with silicide, and the default electron Schottky barrier, *eSBH* = 0.6 eV (NiSi). [5] The DS at source is p-type and the DS at drain is n-type. The DS length, L_{seg} varies from 6 to 20 nm, with 6 nm as default, and the DS doping, N_{seg} varies from 10^{19} to 10^{20} cm^{-3}, with 10^{20} cm^{-3} as default. For both devices, the drain voltage, V_{dd} = 0.5 V, and the default gate work function, *GWF* = 4.175 eV. Work function engineering is applied to get proper voltage bias.[6] In this paper, Synopsys Sentaurus TCAD tools are used for numerical simulation. For TFET, band-to-band tunneling model is applied near source and channel region. For STFET, we add Wentzel–Kramers–Brilliouin (WKB) model to calculate the current through the Schottky barrier. Hydrodynamic model, Fermi distribution and density gradient quantization model are also included in this work.

3. Results and discussion

The electrostatic potential distributions of TFET and STFET are displayed in figure 2. It can be seen that TFET and STFET have similar change rate in the channel region, which shows DS regions can get the same effect as highly doped S/D. Figure 3 shows the electron current density distributions at V_g = 1 V along (a) TFET's and (b) STFET's channel, respectively. TFET has high current density at drain side, and STFET's current density is closer to channel surface. The current density of STFET is lower than that of TFET because of the existence of SB at source contact.

Fig. 4 displays the transfer curves of TFET and STFET. There are different N_{seg} at source side for STFET, while N_{seg} at drain side keeps 10^{20} cm^{-3}. The Off-state current is fixed at 10^{-15} A/μm, and V_{on} = V_{off} + V_{dd}. TFET exhibits the best *SS* and the highest I_{on}. The characteristics of STFET becomes better when N_{seg} at source side increases. Fig. 5 explains this phenomenon by illustrating the electrostatic potential distributions near channel surface. The potential axis is reversed so that we can treat it as energy band. For both devices, the potential changes dramatically at 6 nm from source contact, which is exactly where band-to-band tunneling happens. For TFET, the potential at source is plat, thus providing more drive current. For STFET, there is a hole SB at source side and an electron SB at drain side. When N_{seg} at source is higher, the energy level for p-type DS is lower, so the *hSBH* is higher and the potential change rate at channel/source interface are also supposed to be higher, thus showing better switching characteristics.

In Fig. 6, the transfer curves of TFET and STFET are shown. STFET has different N_{seg} at drain side, while N_{seg} at source side keeps 10^{20} cm^{-3}. The *GWF* for STFET is increased by 0.09 eV for comparison. Here, we can see STFET has similar On-state current because N_{seg} at source is constant. It is also shown that STFET has bipolar behaviors. When N_{seg} at drain increases, the current at V_g = 0 V decreases. Fig. 7 explains this phenomenon by illustrating the electrostatic potential distributions when V_g = 0 V. When N_{seg} at drain is higher, the energy level for n-type DS is higher, so the electron *SBH* is higher. As a result, the electron current of STFET is suppressed.

Fig. 8 shows the influence of $L_{s/d}$ and L_{seg} on TFET's and STFET's performance. When $L_{s/d}$ and L_{seg} changes, the values of STFET and TFET keep almost unchanged, which shows the special characteristics of band-to-band tunneling. It is also found that TFET has higher I_{on} and slightly better *SS* than STFET. In Fig. 9, the relation between I_{on} and *eSBH* is displayed. When *eSBH* at source side is fixed, I_{on} keeps constant when *eSBH* at drain varies. When *eSBH* at both sides increases, I_{on} increases because *hSBH* at source side is smaller. Fig. 10 shows similar phenomenon for *SS* as I_{on} in Fig. 9. When *eSBH* at source side is fixed, *SS* keeps constant when *eSBH* at drain varies. As *eSBH* at both sides increases, *SS* decreases because of a smaller *hSBH*. In Fig. 11, we display the relation between I_{on} and *SS* for TFET and STFET. When T_{si} increases, I_{on} decreases because of less gate control. It is also shown that STFET with L_{seg} = 6, 8, 10 nm has the same I_{on}.

4. Conclusion

In this paper, the characteristics of STFET have been simulated and analyzed. It is found that STFET has I_{on} and *SS* close to TFET's despite the existence of SB. TFET's and STFET's performance are insensitive to L_{seg} and $L_{s/d}$. High N_{seg} is necessary for STFET to reach high voltage difference at source/channel interface for band-to-band tunneling. STFET demands high N_{seg} to build high barrier at drain side to eliminate bipolar behaviors. Moreover, increasing *eSBH* at source side is beneficial to increasing I_{on} and *SS*, while the change of *eSBH* at drain side has almost no influence to the performance at On-state.

Acknowledgement

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Reference

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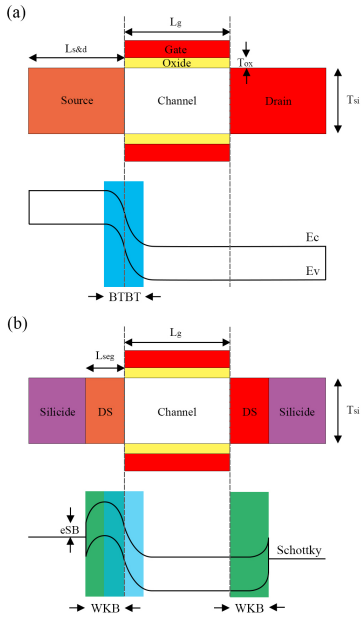

Fig. 1 Schematic structures and energy band diagrams of (a) TFET and (b) STFET.

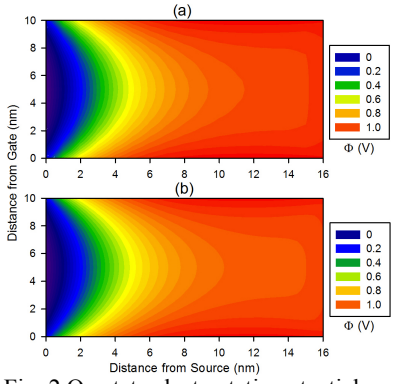

Fig. 2 On-state electrostatic potential distributions: (a) TFET and (b) STFET.

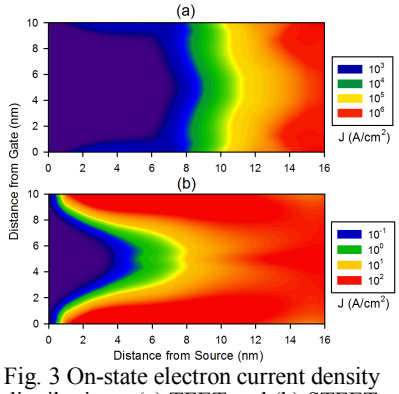

Fig. 3 On-state electron current density distributions: (a) TFET and (b) STFET.

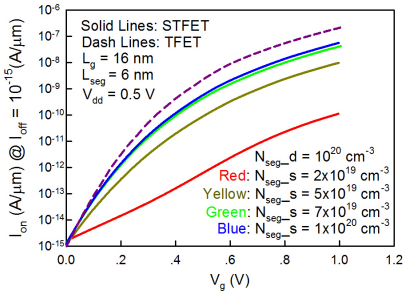

Fig. 4 Transfer curves of TFET and STFET with different N_{seg} at source side. V_{dd} = 0.5 V, and I_{off} is fixed at 10^{-15} A/μm.

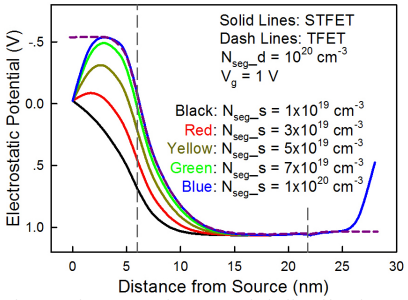

Fig. 5 Electrostatic potential distributions 0.625nm from channel surface. V_g = 1 V.

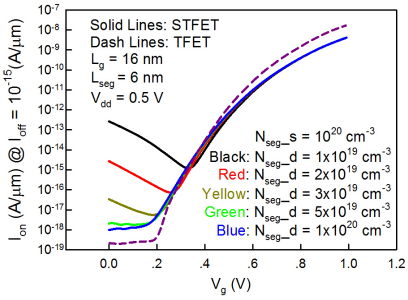

Fig. 6 Transfer curves of TFET and STFET with different N_{seg} at drain side. V_{dd} = 0.5 V, and *GWF* for STFET is 4.265 eV.

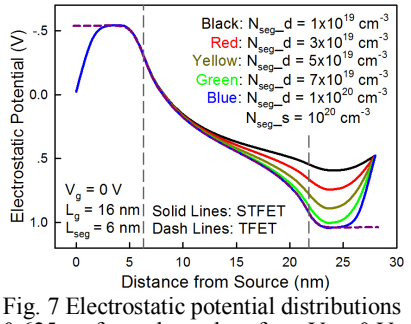

Fig. 7 Electrostatic potential distributions 0.625nm from channel surface. V_g = 0 V.

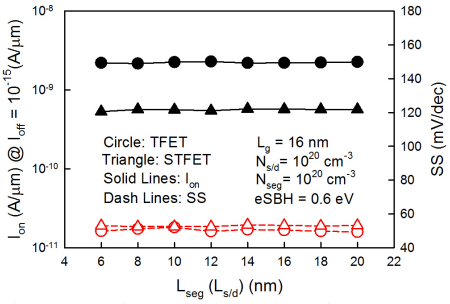

Fig. 8 I_{on} and *SS* versus L_{seg} ($L_{s/d}$) for TFET and STFET. V_{dd} = 0.5 V, and I_{off} is fixed at 10^{-15} A/μm.

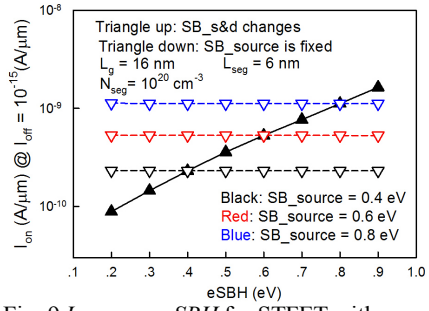

Fig. 9 I_{on} versus *eSBH* for STFET with fixed *SBH* at source side. V_{dd} = 0.5 V, and I_{off} is fixed at 10^{-15} A/μm.

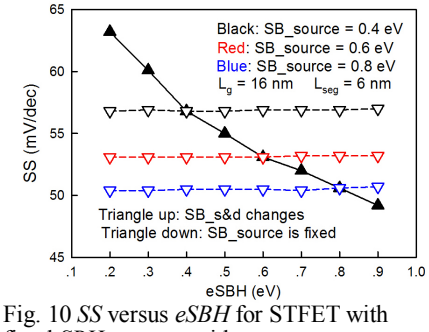

Fig. 10 *SS* versus *eSBH* for STFET with fixed *SBH* at source side.

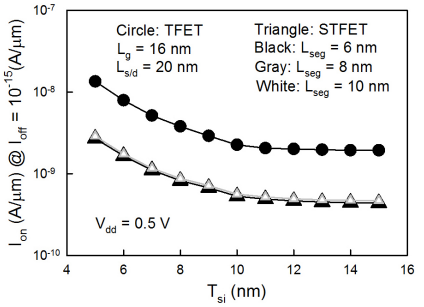

Fig. 11 I_{on} versus T_{si} for TFET and STFET. V_{dd} = 0.5 V, and I_{off} is fixed at 10^{-15} A/μm.