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RF Characteristics of Poly-Si TFTs with HfO_2 Gate Dielectric Fabricated by Microwave Annealing

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Abstract

This work presents the RF characteristics of the poly-Si TFTs with high-κ HfO_2 gate dielectric annealed by low-temperature MWA. The cutoff frequency (f_T) and oscillation frequency (f_{max}) of poly-Si TFTs with different layout structures, including annular, single, and parallel are investigated. The annular layout structure with L=150 nm has a higher f_T (1.69 GHz). Results show that the poly-Si TFT technique can feasibly be utilized in system-on-panel applications.

1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have higher electron mobility and driving current than amorphous silicon TFTs and have potential for RF applications [1-3]. The RF performance is expected to improve with scaling. However, continuous shrinking of device is facing several challenges, such as short channel effects (SCEs) and high gate leakage current. It has been reported that low-temperature microwave annealing (MWA) technique can restrain the dopant diffusion and suppress the short channel effects [4-5]. In addition, poly-Si TFTs with high-κ gate dielectric have been proposed to have lower gate-leakage current and better electrical characteristics than with SiO_2 gate dielectric [6-7]. Therefore, in this work, poly-Si TFTs with high-κ HfO_2 gate dielectric annealed by MWA are fabricated. The high-frequency characteristics of poly-Si TFTs with different layout structures are studied.

2. Experiments

Fig. 1 shows the top-view SEM images of poly-Si TFTs with different layout structures, including annular, single, and parallel. The gate length (L) of poly-Si TFTs are 105 nm as shown in Fig. 1(d). The total gate-width of devices in this work are fixed at 44 μm for comparison. A 100-nm thick layer of active is a solid-phase-crystallized poly-Si film. A 50-nm thick TiN layer and a 4-nm-thick HfO_2 layer act as the metal gate electrode and gate dielectric, respectively. Low-temperature MWA for dopant activation is performed at 3 kW for 300 sec.

3. Results and Discussion

Fig. 2 shows I_{DS}-V_{GS} transfer curves of poly-Si TFTs with different layout structures. The DC characteristics of these three structures are similar. In Fig. 3, the cutoff frequency (f_T) of the annular one is obviously higher than the others. Since the usual approximation for f_T is $g_m/2\pi(C_{gs}+C_{gd})$, the small-signal parameters are extracted and analyzed. Fig. 4 and Fig. 5 show the extracted transconductance (g_m) and gate parasitic capacitances (C_{gs}, C_{gd}) for all devices. Although the g_m value of the annular one is not the highest, the C_{gs} and C_{gd} of the annular one are the smallest. Therefore, the annular one has the highest f_T. In Fig. 5, the parallel one has higher C_{gs} and C_{gd} than the single one due to stripe-shape gate configuration. Hence, the better f_T of the parallel one than of the single one is attributed to the higher g_m in the parallel one than in the single one. Fig. 6 shows the oscillation frequency (f_{max}) of all devices. The approximation for f_{max} can be expressed as follows [8]:

$$f_{max} \sim \frac{f_T}{\sqrt{4g_{DS}R_g + 8\pi f_T C_{gd}(R_g + \alpha R_d)}}$$

The f_{max} is proportional to the f_T and is strongly related to the gate resistance (R_g). The extracted R_g for all devices is show in Fig.7. Although the R_g value of the annular one is not the lowest, the f_T of the annular one is the highest. Therefore, the annular one has the highest f_{max}. As for the single and parallel layout structures, with a constant total gate-width, the R_g values decrease as the finger width increase. Hence, the parallel one has higher f_{max} than the single one. Fig. 8 shows the peak f_T values of all devices before and after sintering. The enhanced f_T after sintering is attributed to the passivation of grain boundary defects and poly-Si/interfacial oxide interface states [7]. After sintering, the peak f_T of the annular one with L = 150 nm is 1.69 GHz.

4. Conclusions

The high-frequency performance of poly-Si TFTs with HfO_2 gate dielectric annealed by MWA are investigated. The annular layout structure exhibits higher f_T and f_{max} than the other layout types. Additionally, poly-Si TFT with L = 105 nm still has acceptable switching characteristics due to low-temperature MWA which restrain the dopant diffusion. Consequently, the RF performance can be improved by shrinking the gate length in conjunction with MWA.

References

[1] J. L. Botrel *et al.*, *Thin Solid Films* **515** (2007) 7422.
[2] Y. J. E. Chen *et al.*, *IEEE Trans. Microw. Theory Tech.* **58** (2010) 3444.
[3] S. Y. Kim *et al.*, *IEEE Trans. Electron Devices* **59** (2012) 2296.
[4] T. L. Alford *et al.*, *J. Appl. Phys.* **106** (2009) 114902.
[5] Y. J. Lee *et al.*, *IEEE Electron Device Lett.* **34** (2013) 1286.
[6] Chia-Pin Lin *et al.*, *IEEE EDL.* **27** (2006) 360.
[7] Chen-Ming Lee *et al.*, *IEEE EDL.* **32** (2011) 327.
[8] T. C. Lim *et al.*, *Solid-State Electron*. **50** (2006) 774.

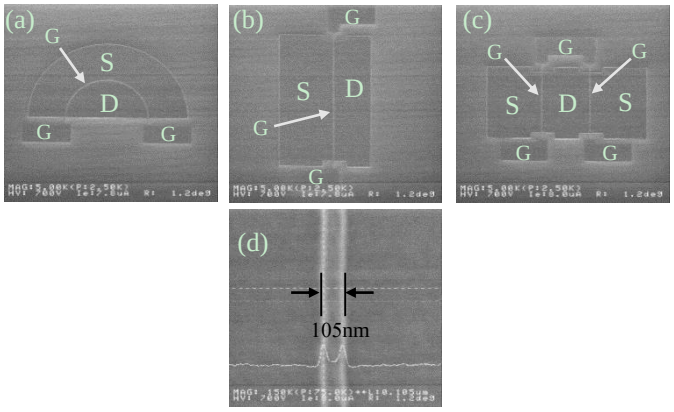

Fig. 1 Top-view SEM image of (a) annular, (b) single, (c) parallel, and (d) active region of poly-Si TFT with L= 105 nm.

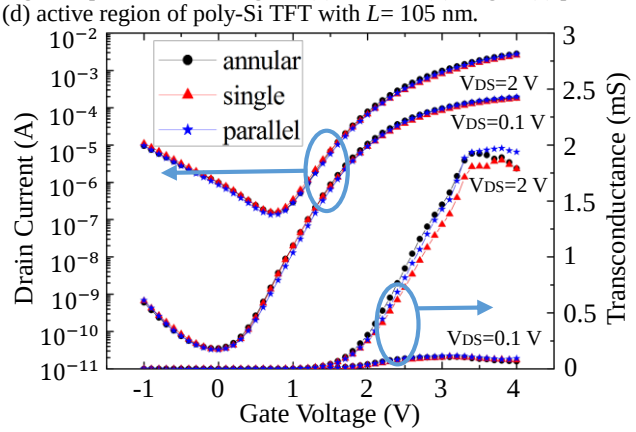

Fig. 2 The $I_{DS} - V_{GS}$ transfer curves with different layout structures.

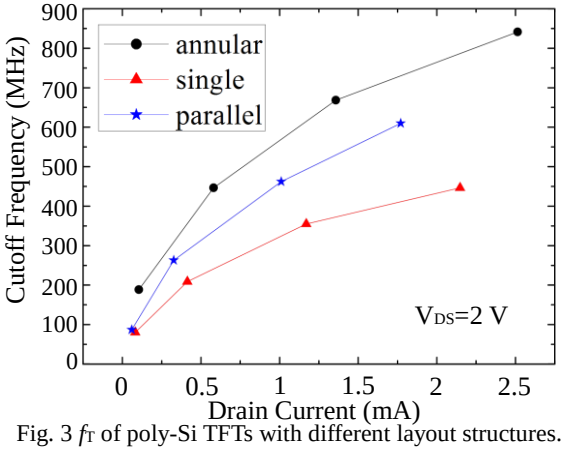

Fig. 3 f_T of poly-Si TFTs with different layout structures.

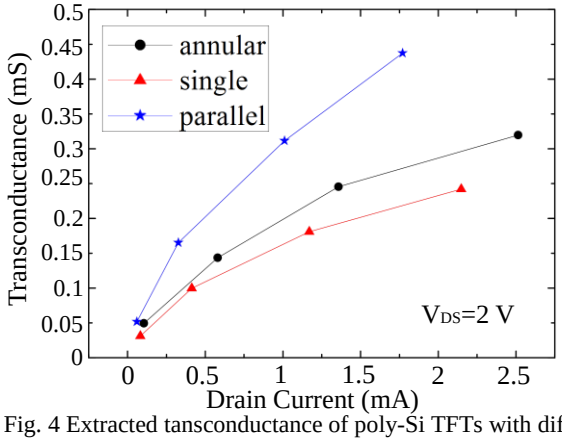

Fig. 4 Extracted tansconductance of poly-Si TFTs with different layout structures.

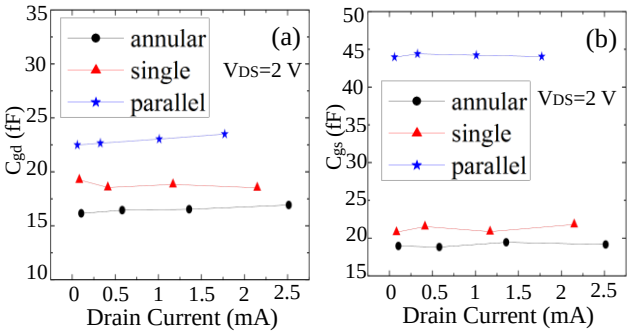

Fig. 5 Extracted (a) C_{gd} and (b) C_{gs} of poly-Si TFTs with different layout structures.

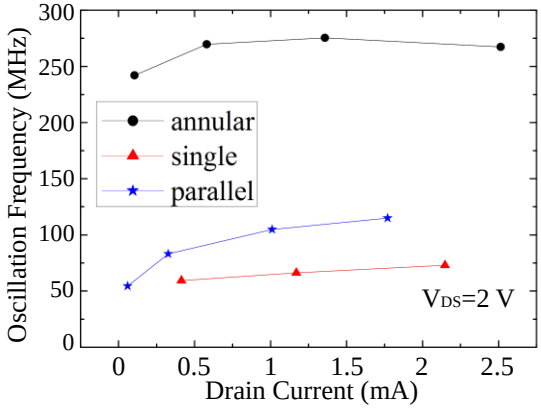

Fig. 6 f_{max} of poly-Si TFTs with different layout structures.

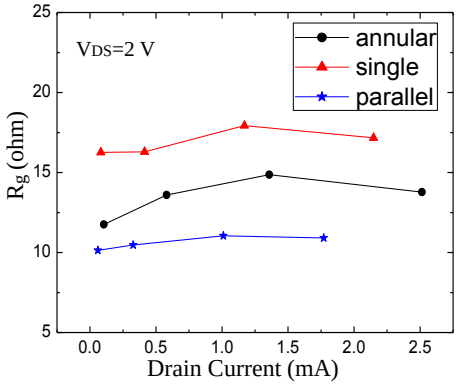

Fig. 7 Extracted R_g of poly-Si TFTs with different layout structures.

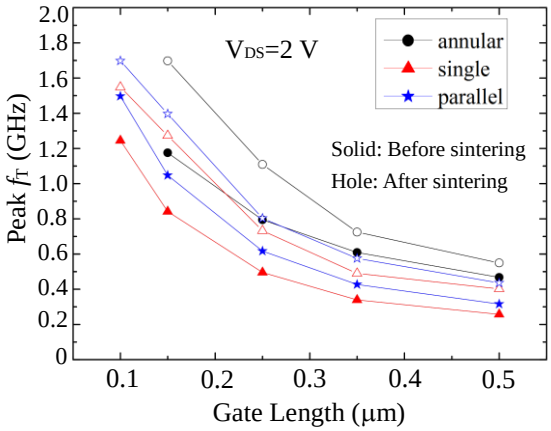

Fig. 8 Nonsintered and sintered peak f_T of poly-Si TFTs with different layout structures.