Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp94-95

Comparison of Gate Structures of P-channel Poly-Si Nanowire Trench Ultra-thin Channel Juntionless Field-Effect Transistors

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Abstract ~ This work demonstrates P-channel Poly-Si trench junctionless field-effect transistor (JL-FET) with ultra-thin channel (UTC), adopted easily dry etching process. Two kinds of gate structure, G_{out} and G_{in} JL-FET with UTC thickness (T_{CH}) of 5.7 nm and effective gate length (L_G) of 0.6 μm are comparison. The G_{out} device shows excellent performance with a steep subthreshold slope (SS~111 mV/dec.), low drain induced barrier lowering (DIBL~0), and high I_{ON}/I_{OFF} (>10^8), owing to excellent gate control to UTC and benefit of raised source/drain. Gin device has high density advantage.

1. Introduction

Scaling down of the IC devices and 3D stacked devices are current urgent studies. Nowadays, the CMOS reliable junction formation is still heavy challenge when the devices are continuously scaling down. Therefore, JL-FET seems the way to surmount the problem [1]-[5]. For the JL-FET, the channel thickness is the most critical parameter, which needs to be thin enough to deplete the heavily doped channel. In this work, the dry etching process is utilized for fabrication of trench JL-TFT. It forms a UTC and also defines the channel thickness (T_{CH}) and the gate length (L_G) [1],[3]. We compare two gate structures devices' electrical performance. One is gate electrode covering whole trench called Gate-out (G_{out}) structure JL-FET (Fig. 1a), another is gate electrode inside the trench called Gate-in (G_{in}) structure JL-FET (Fig. 1b).

2. Experiment

Fig. 1c shows the process flow of trench JL-FET. First, 40-nm-thick poly-Si film is formed. Then, poly-Si layer was implanted BF_2 ions at a dose of 2×10^{14} cm^{-2}. The channel nanowires (NWs) were defined by e-beam lithography (EBL) and transferred by reactive-ion etches (RIE) [1]. The UTC trench structure was also patterned by EBL and time-controlled RIE. Subsequently, an 8-nm-thick dry oxide was growth as the gate oxide layer. Furthermore, 150-nm-thick in-situ doped n^+ poly-Si deposited as the gate electrode, and patterned by EBL and RIE. Finally, the metallization was performed.

3. Results and Discussion

Fig. 2a & 2b show the scanning electron microscope (SEM) images trench JL-FET for G_{out} and G_{in} devices, respectively. G_{out} device controls more active region. G_{in} device has small device area. Fig. 2c & 2d show atomic force microscope (AFM) images of active channel with ten NWs and its trench structure. Fig. 3a and 3b show transmission electron microscopic (TEM) images for G_{in} and G_{out} devices, respectively. Fig. 3c shows TEM image along gate direction, which is formed the Ω-gate structure. The device's effective width (W_{eff}) is 90 nm×10, effective L_G is 0.6 μm and T_{CH} is 5.7 nm.

Fig. 4 shows the I_D-V_G curves of G_{out} and G_{in} trench JL-FETs with L_G=0.6μm. The G_{out} device has a steeper SS (111 mV/dec.) and a lower DIBL (5 mV/V) than that of the G_{in} device. G_{out} and G_{in} devices have a favorable threshold voltage (V_{TH}) with -1.28 and -1.71 V, respectively. The V_{TH} is defined of V_G at $I_D = 10^{-9}$A. The G_{out} device has higher I_{on} and I_{off} than that of G_{in} device.

Fig. 5 shows the I_D-V_G and transconductance (g_m) characteristics of G_{out} and G_{in} trench JL-FET with the same effective L_G=0.6μm. The G_{out} device has a higher maxima g_m than G_{in} device, owing to more channel control area (Fig. 2a) and the benefit of effective raised source/drain.

Fig. 6 shows the total resistance (R_{total}) of G_{out} and G_{in} devices as a function of gate voltage. The relationship between the S/D series resistance (R_{SD}) and the R_{total} are described in the inset of Fig. 5. R_{total} is inversely proportional to mobility. G_{out} device has low slope and reveals G_{out} with a high mobility.

Fig. 7 compares the I_D-V_D output characteristics of the G_{out} and G_{in} trench JL-FET for L_G = 0.6 μm. G_{out} device has higher saturation current than G_{in} device. It is consistent with more channel control area and the benefit of effective raised source/drain of G_{out} device. Fig. 8a & 8b show temperature dependence of I_D-V_G curves for G_{out} and G_{in} devices, respectively. The I_{on} and V_{TH} exhibit positive and negative shifting with the temperature increasing, respectively.

4. Conclusion

This study comparison performance of G_{out} and G_{in} trench JL-FET with UTC. The G_{out} device has better electrical performance than that of G_{in} device due to more channel area control. On the contrary, G_{in} device has high density advantage. The proposed trench JL-FET with UTC is easy fabricated and compatible with current CMOS technologies. which are promising for applications in nano-scale device and 3-D stacked device applications.

Acknowledgements

We thank Taiwan National Science Council (NSC) under Contract MOST 103-2221-E-007-114-MY3 support and NDL of Taiwan for technical support.

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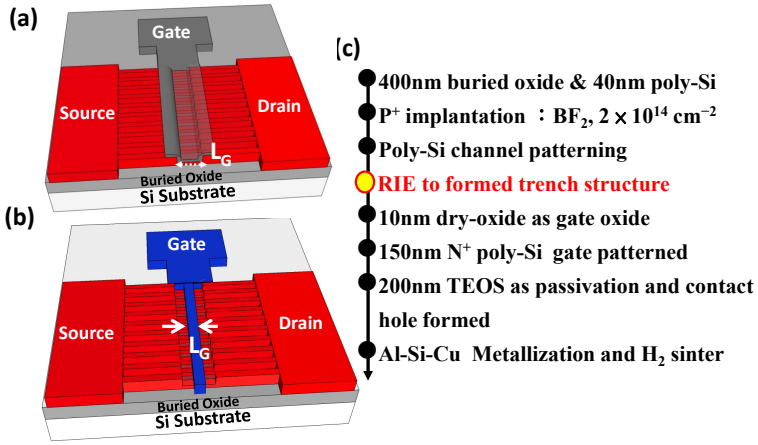

Fig. 1. (a) G_{out} structure and (b) G_{in} structure trench JL-FET devices. (c) Process flow chart of the theses devices fabrication.

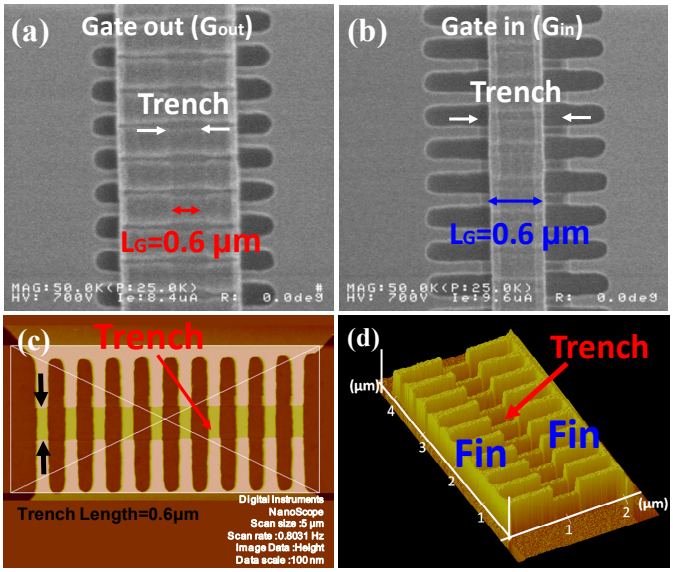

Fig. 2. Top-view SEM image of trench JL-FET for (a) G_{out} and (b) G_{in} structures with effective L_G=0.6μm. G_{out} device controls more active region. G_{in} device has small device area. (c) & (d) are AFM images of active channel region of trench JL-FET with ten NWs.

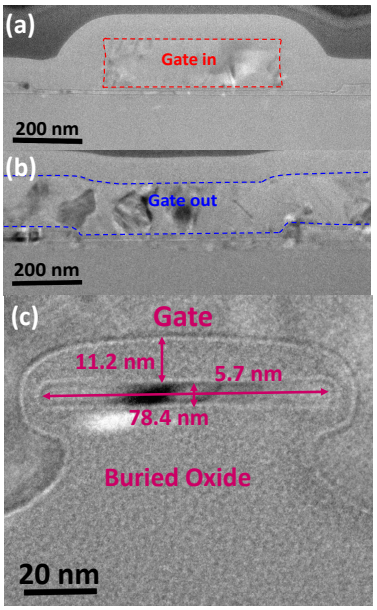

Fig. 3. TEM images for (a) G_{in} and (b) G_{out} structure trench JL-FET with effective L_G=0.6μm. G_{out} device controls more active region. G_{in} device has small device area. (c) TEM image along gate direction to form the Ω-gate structure. W_{eff} =(78.4nm+5.7nm×2) ×10=90nm×10

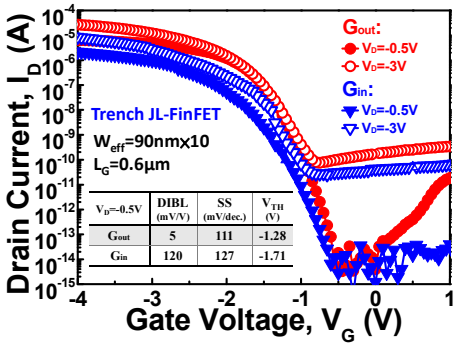

Fig. 4. Comparison of the I_D-V_G curves of G_{out} and G_{in} NWs trench JL-FET with L_G=0.6 μm at V_d= -0.5V and -3V. The G_{out} device has higher I_{on} and I_{off} than that of G_{in} device.

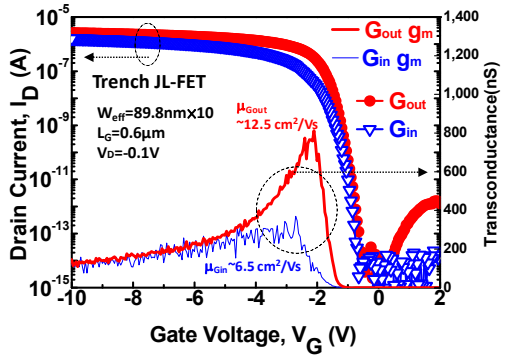

Fig. 5. I_D-V_G curves of G_{out} and G_{in} trench JL-FETs with L_G=0.6μm. The G_{out} device has a higher g_m and μ, owing to more channel control area (Fig. 2a) and the benefit of effective raised source/drain.

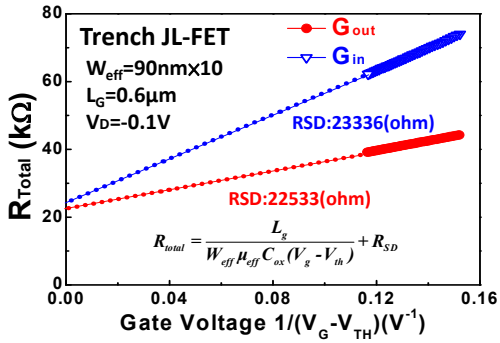

Fig. 6. R_{total} for G_{out} and G_{in} trench JL-FETs with L_G=0.6 μm.

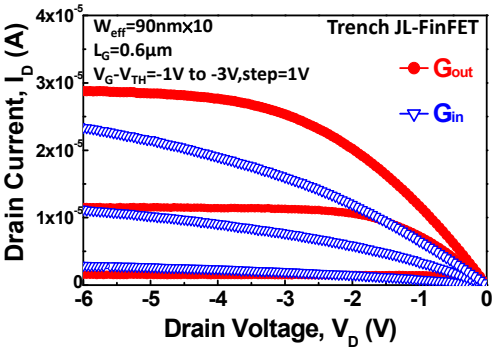

Fig. 7. I_D-V_D curves of G_{out} and G_{in} trench JL-FET with L_G=0.6μm.

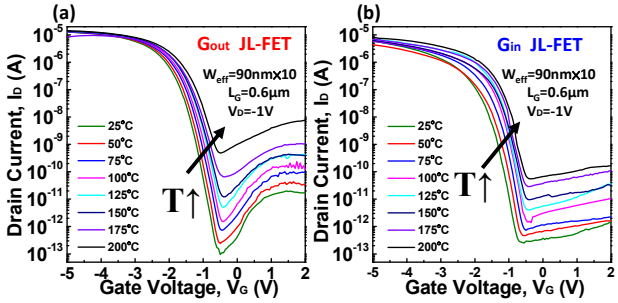

Fig. 8. Temperature dependence on I_D-V_G curves of G_{out} and G_{in} devices.