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ON current Enhancement of Nanowire Schottky Barrier Tunnel FET

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Abstract

We demonstrate that the ON current density of silicon nanowire Schottky barrier tunnel FET (NW-SBTFET) is enhanced by narrowing the width of the nanowire. The ON current mainly comprises the quantum tunneling component through the Schottky barrier, which is confirmed by the Fowler-Nordheim plot. Comparison with a TCAD simulation reveals that the enhancement is attributed to the electric field concentration at the corners of cross-section of the nanowire.

1. Introduction

Schottky barrier (SB) FET has recently attracted attention by the demonstration of a very steep subthreshold slope of 3.4mV/dec [1] and the ability to boost the ON current of band-to-band tunnel FET [2]. The ON current is sustained by the tunneling through the SB between source and channel, so that the enhancement of the tunneling current has a significant impact on the practicalization of these devices.

In this work, we fabricated a silicon nanowire Schottky barrier tunnel FET (NW-SBTFET) to investigate the effect of nanowire structure on the device characteristics. We have found that the ON tunneling current is significantly enhanced in narrower NWs.

2. Experiment

Fig.2 shows fabrication process flow of NW-SBTFET. The device is fabricated on lightly p-type doped (100)SOI wafer with 45nm thick Si and 145nm thick BOX. <110> oriented Si-NWs of 10 lines and pads are fabricated by EB-Lithography, TMAH etching and thermal oxidation in dry O_2 ambient at 850℃ for 3h. The NWs are connected to the electrode pad. The NW width (W) including the oxide shell is 68nm~120nm. After oxidation, P ions are implanted at 25keV with a dose of 1.0×10^{12}cm^{-2}. The drain side pad is implanted with 25keV P to a dose of 1.0×10^{15}cm^{-2} and activated at 950℃ for 10min to form an ohmic contact. The oxide layer is partially removed by BHF and 20nm thick Ni is deposited by ion sputtering. Then Ni silicide is formed by annealing at 410℃ for 120s. The unreacted Ni is removed by SPM. Finally, the oxide on the drain side pad is removed by BHF and AlSi electrodes are formed on source/drain pads.

The schematic of the device structure is shown in Fig.3(a). Fig.3(b) and 3(c) show the SEM image of Ni silicided NW and cross-sectional SEM image of Si-NWs, respectively. FET operation is carried out by applying the backgate voltage (V_{bg}).

3. Results and Discussions

Fig.4(a) shows I_d-V_d characteristic without applying V_{bg}, which corresponds to the Schottky diode characteristic of the source-channel contact. The forward bias current is extrapolated to zero volt to obtain the thermionic emission current J_s (inset of Fig.4(a)) expressed by the Rechardson-Dushman equation, and the effective Schottky barrier height(SBH) Φ_{Bn} and ideal factor n are obtained as shown in Fig.4(b) and Fig.4(c), respectively, using thermionic emission model. SBH is estimated to from 0.50 to 0.60 eV, which is lower than the literature SBH of 0.67eV [3] for planer NiSi/Si interface. Ideal factor value increases as the NW narrows.

Fig.5(a) shows I_d-V_{bg} characteristic of NWs of 120 nm wide. I_d increases exponentially with V_{bg}. I_d-V_{bg} characteristics for 68nm and 120nm wide NWs are shown in Fig.5(b), showing that the ON current density is enhanced in the narrower NW devices. The Fowler-Norheim(F-N) pot [4,5] for various V_{bg} is shown in Fig.6(a). A negative slope appears in the range of $V_{bg} > 20$V. Fig.6(b) shows the temperature dependency of the F-N analysis. There is no temperature dependence of the negative slope, suggesting that a F-N tunneling through the SB is the dominant in the range of $V_{bg} > 20$V .

ON current density enhancement observed in narrower NW devices can be attributed to (1) the increase in the tunneling current by the trap-assisted tunneling(TAT) or (2) Schottky barrier width(SBW) modulation due to the electric field concentration at NW edge.

In order to investigate the effect of (1) TAT, we carried out the 2-D TCAD simulation [6]. Universal Schottky [7] model and Schenk model [8] are employed to reproduce the Schottky barrier tunneling(SBT) and TAT, respectively (Fig. 7). The simulated device structure and the device parameters are set as shown in Fig.8 and Table.1, respectively. Fig. 9 shows the calculated I_d-V_{bg} characteristic together with the experimental result. Although the TAT current plays an important role to reproduce the subthreshold characteristics, it does not contribute to ON current density, as reported in a previous work on band-to-band tunnel FET [9].

Next, we investigate the (2) SBW modulation due to the electric field concentration by analyzing the electric field distribution of NWs as shown in Fig.10. Electric field is

concentrated at the NW edges, the extent is larger in the narrower NWs. Thus, we conclude that the ON current density is mainly enhanced by electric field concentration.

4. Conclusions

We have found that the ON current density observed in narrow NW-SBTFET is enhanced by the electric field concentration. Thus, the merit of the NW geometry can be exploited more effectively by controlling the tunneling current through the Schottky barrier. A rectangular cross-section of NW is considered to be more preferable than circular one to maximize the SBW modulation effect.

Acknowledgements

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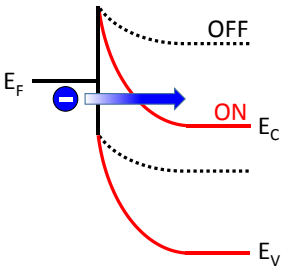

Fig.1 Schematic of energy band diagram of SBTFET.

- (100) SOI wafer(t_{SOI}=45nm, t_{BOX}=145nm)
- Thermal oxidation(850℃, 3h, t_{OX}=18nm)
- Pads & [110]NWs patterning
- Thermal oxidation(850℃, 3h, t_{OX}=18nm)
- Ion Implantation(P^+, 25keV, 10^{12} cm^{-2})
- Ion Implantation(P^+, 25keV, $10^{15}cm^{-2}$)
- Dopant activation RTA(950℃, 10min)
- Ni depo.(t_{Ni}=20nm)
- Silicidation annealing(410℃, 120s)
- AlSi electrode depo.(t_{AlSi}=300nm)

Fig.2 Process flow of SBTFET.

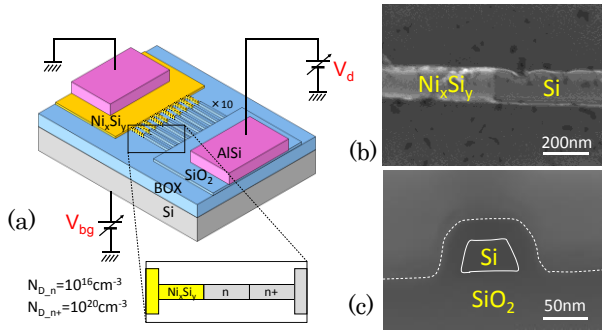

Fig.3 (a) Schematic of SBTFET, (b) SEM image of Ni slicided NW, (c) SEM image of cross-sectional NW.

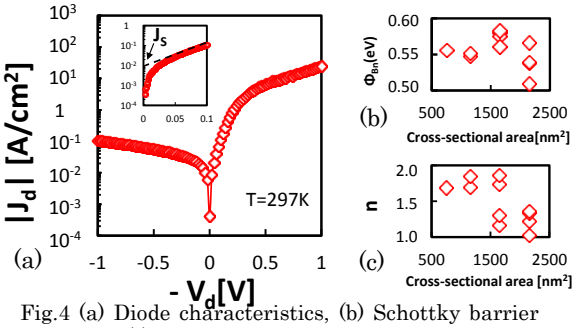

Fig.4 (a) Diode characteristics, (b) Schottky barrier height Φ_B, (c) ideal factor n.

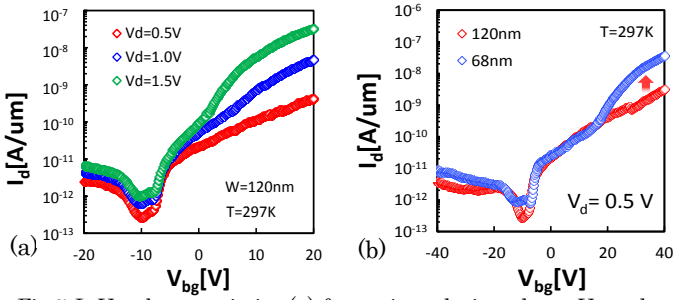

Fig.5 I_d-V_{bg} characteristics (a) for various drain voltage V_d and (b) with different NW width.

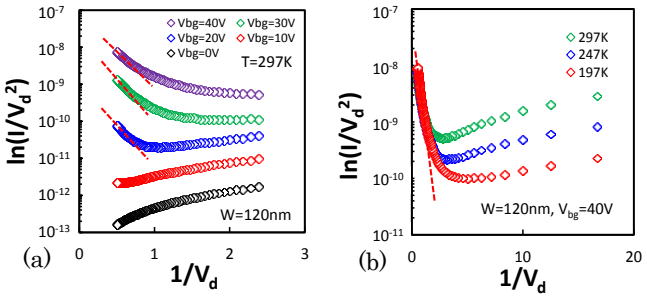

Fig.6 F-N plot for (a) various backgate voltage V_{bg} and (b) various temperature.

Table.1 Device parameters used in the simulation.

Drain voltage [V]	2.0
Work function [eV]	4.70
Doping density(n) [cm^{-3}]	1.0×10^{16}
Doping density(n^+) [cm^{-3}]	6.5×10^{20}
Trap density [cm^{-3}]	4.0×10^{17}
Trap level [eV]	0.9
Contact resistance[kΩ]	2500

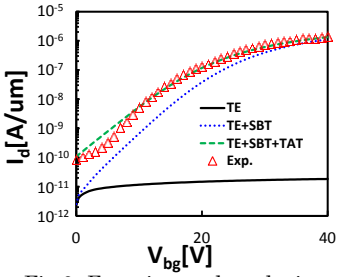

Fig.9 Experimental and simulated I_d-V_{bg} characteristics.

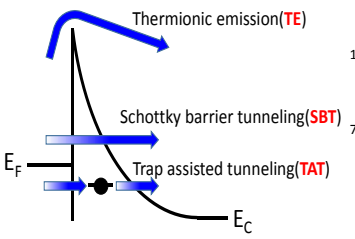

Fig.7 Schematic of current component.

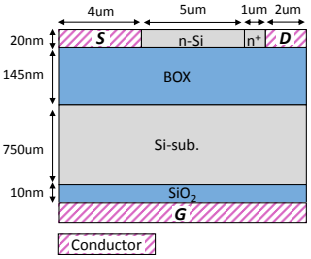

Fig.8 Schematic of simulated device structure.

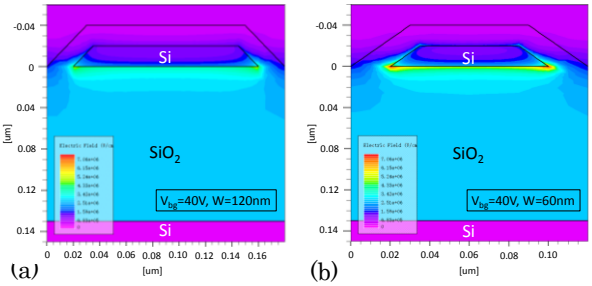

Fig.10 Simulated electric field distribution for V_{bg}=40V with NW width of (a) 60nm and (b) 120nm.