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Novel 5-State Latch Using Double-Peak Negative Differential Resistance (NDR) and Standard Ternary Inverter (STI)

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1. Introduction

The multi-valued logic (MVL) and memory (MVM) are the promising solutions for bit density limits of conventional binary logic-based integrated circuit [1]. As an alternative device for MVL/MVM, the negative differential resistance (NDR) devices have received much attentions owing to its non-monotonic behaviors, however, its low peak-to-valley current ratio (PVCR) or CMOS incompatible process restrict practical applications [2]. Even though many research works enhance the performance of single-peak NDR devices based on CMOS compatible structure, the complicated circuit compositions for multi-peak NDR and its logic gate still remained as problems [3]. In our previous work, complementary double-peak NDR device with ultra-high PVCR over 10^6 proposed, and 5-state latch with positive and negative ternary inverter (PTI and NTI) was demonstrated [4]. In this work, we propose a novel 5-state latch with double-peak NDR device and standard ternary inverter (STI) using only 4 devices.

2. Operation principle of 5-state latch

Figure 1(a) shows the 5-state latch circuit configuration with *n*-type NDR (*n*NDR), *p*-type NDR (*p*NDR), and CMOS STI (*n*MOS and *p*MOS). For the double-peak NDR characteristics, the degenerately doped *pn* tunnel junction is embedded at drain side of simple MOSFET structure as shown in Fig. 1(b) [4]. The 1st NDR characteristics is obtained by band-to-band tunneling (BTBT), trap-assisted tunneling (TAT), and diffusion as in a normal tunnel (Esaki) diode with on-state MOSFET, while the 2nd NDR characteristics is achieved by off-state MOSFET which inhibit the flow of electrons with high channel potential barrier. The front circuit of Fig. 1(a), CMOS STI, is introduced for single input sweep between gate and drain (V_G and V_D=V_{IN}), complementary double peak NDR curves of *n*/*p*NDR, and 5-state latch with the same unit cell area of binary latch circuit. To generate the additional intermediate state of STI based on conventional binary inverter circuit, we used V_{IN} independent junction BTBT currents as dominant off current mechanism with high channel doping concentration (Fig. 1(c)) [5]. When both *n*/*p*MOS flow the constant off currents with similar trans-conductance, the intermediated state is determined by voltage dividing between *n*/*p*MOS.

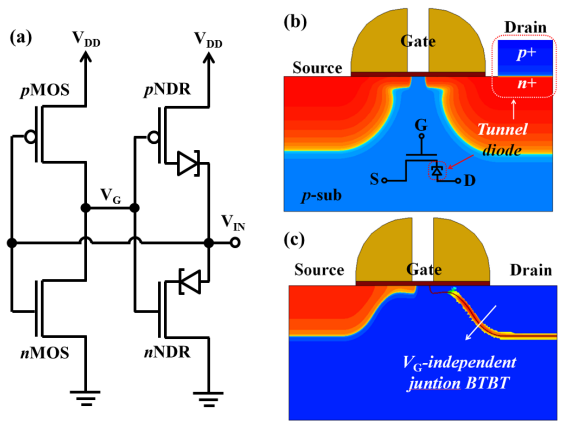
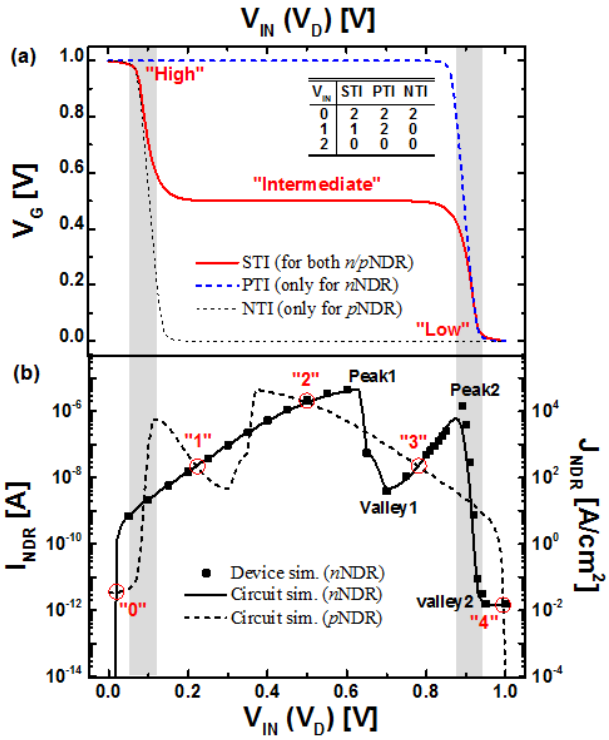


Fig. 1 (a) 5-state latch circuit composed with CMOS STI (*n*MOS and *p*MOS), *n*-type NDR (*n*NDR), and *p*-type NDR (*p*NDR) (b) 2-D cross sectional view and circuit symbol of *n*NDR [4] (c) 2-D cross section view and band-to-band generation view of *n*MOS for STI [5].



V_{IN}	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

Fig. 2 (a) Simulated voltage transfer curve (VTC) of CMOS STI/PTI/NTI (b) complementary NDR characteristics of *n*NDR and *p*NDR based on Fig. 1(a)

Figure 2(a) and (b) show the voltage transfer curve (VTC: V_G-V_{IN}) of STI/PTI/NTI and successive complementary NDR characteristics (I_{NDR}-V_{IN}) with ultra-high PVCR over 10^6 at V_{DD}= 1V based on proposed operation

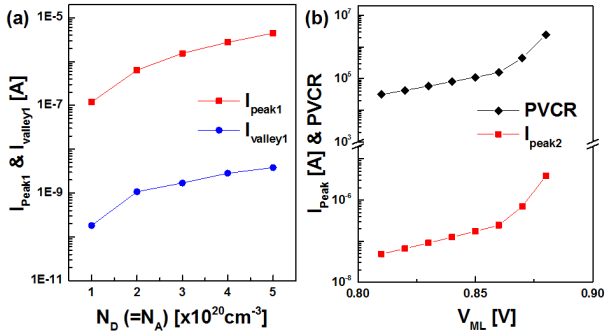


Fig. 3 (a) peak1 and valley1 currents according to doping concentration of *pn* tunnel diode (b) peak2 currents and 2nd PVCR according to transition voltage (V_{ML} @V_G=V_{DD}/4) of STI.

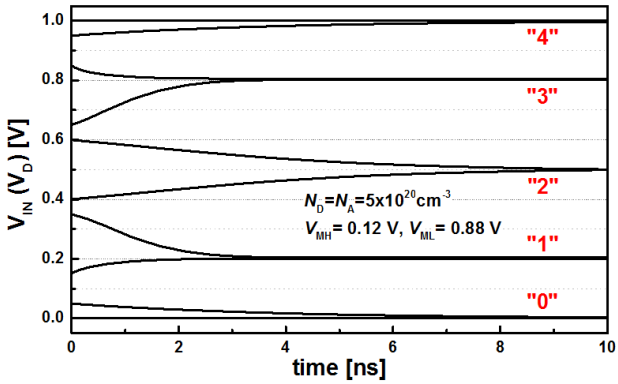


Fig. 4 Transient simulation results of the latch circuit. Initial states of V_{IN} with variation of ±100mV are converged to 5-states.

principle where the 1st peak (peak1) and 1st valley (valley1) are generated by a typical tunnel diode behavior and the subsequent 2nd peak (peak2) can be formed by suppressing the 2nd valley (valley2) at the MOSFET off-leakage level. The STI can be suppressed the 2nd valley (valley2) current with complementary V_G for each multiple *n*NDR (V_G= 0 V) and *p*NDR (V_G =1V), whereas PTI or NTI can be applied on only for multiple *n*NDR or *p*NDR, respectively. The intermediate state (V_G =0.5V) of STI plays a key role for compact circuit design with 33% area reduction compared with previous work about 5-state latch [4], since it can implement 1st NDR characteristics in both *n/p*NDR devices by supplying the channel electrons to tunnel diode. Moreover, in terms of bit density, 57% reduced number of bit can be obtained compared with binary logic. Device simulation was performed by using Sentaurus^{TM} 3-D TCAD device simulator with our numerical BTBT model in order to describe BTBT mechanism (peak1) in forward bias of tunnel diode [6]. For the valley1 current through a forbidden band-gap, field enhanced TAT model is used [7]. *HSPICE* circuit simulation was performed using BSIM4 model (level 54). By obtaining the peak1 voltage (V_{peak1}) above V_{DD}/2, 9-corssing point between *n/p*NDR obtained as shown in Fig. 2(b). Among of them, 5-crossing points (red circle) in positive differential resistance (PDR) become logic or memory states, while other 4-crossing points in NDR region become boundaries between stable states [8].

3. Results and discussion

Figure 3(a) and (b) analyze the multiple NDR characteristics according to design parameters such as doping concentration of *pn* tunnel diode and VTC of STI. Figure 3(a) shows that the peak1 currents (I_{peak1}) by BTBT and valley1 currents ($I_{valley1}$) by TAT increase by field enhancement when doping concentration of *pn* tunnel junction increases from 1x10^{20} to 5x10^{20} cm^{-3}. In Fig. 3(b), high transition voltage from intermediate to low state (V_{ML}: V_{IN} @ V_G=V_{DD}/4) allows high 2nd PVCR over 10^6 of *n*NDR with exponentially increased peak2 current (I_{peak2} ~ exp(q(V_{GS}-V_T)/mk_BT)) and fully suppressed valley2 current ($I_{valley2}$) at MOSFET off-current level (~1pA), while lower transition voltage from high to intermediate state (V_{MH}: V_{IN} @ V_G= 3V_{DD}/4) increase 2nd PVCR of *p*NDR in a complementary way.

Figure 4 shows the transient simulation results of the latch circuit in Fig. 1(a) having I_{NDR}-V_{IN} characteristics of Fig. 2(b). Initial state of V_{IN} with variation ±100mV are successfully converged to 5 states (marked as "0", "1", "2", "3", "4" in Fig. 4). The speed of "2"-state can be comparable with other states since the stable operating point is crossing around high peak current (not low valley's one), which can be enhanced further by developing the tunnel junction technology with high peak current density.

4. Conclusions

We proposed the novel 5-state latch with only 4 transistors based on CMOS STI and complementary double-peak NDR devices, which facilitates 57% bit density reduction from the binary latch. Multiple NDR characteristics have been investigated with analysis of current component according to the device design parameters and 5-state latch based on multiple NDR characteristics has been successfully demonstrated with circuit simulations.

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