Novel 5-State Latch Using Double-Peak Negative Differential Resistance (NDR) and Standard Ternary Inverter (STI)

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1. Introduction

The multi-valued logic (MVL) and memory (MVM) are the promising solutions for bit density limits of conventional binary logic-based integrated circuit [1]. As an alternative device for MVL/MVM, the negative differential resistance (NDR) devices have received much attention owing to its non-monotonic behaviors, however, its low peak-to-valley current ratio (PVCR) or CMOS incompatibility restricts it practical applications [2]. Even though many research works enhance the performance of single-peak NDR devices based on CMOS compatible structure, the complicated circuit compositions for multi-peak NDR and its logic gate still remained as problems [3]. In our previous work, complementary double-peak NDR device with ultra-high PVCR over $10^6$ proposed, and 5-state latch with positive and negative ternary inverter (PTI and NTI) was demonstrated [4]. In this work, we propose a novel 5-state latch with double-peak NDR device and standard ternary inverter (STI) using only 4 devices.

2. Operation principle of 5-state latch

Figure 1(a) shows the 5-state latch circuit configuration with n-type NDR (nNDR), p-type NDR (pNDR), and CMOS STI (nMOS and pMOS). For the double-peak NDR characteristics, the degenerately doped $p/n$ tunnel junction is embedded at drain side of simple MOSFET structure as shown in Fig. 1(b) [4]. The 1st NDR characteristics is obtained by band-to-band tunneling (BTBT), trap-assisted tunneling (TAT), and diffusion as in a normal tunnel (Esaki) diode with on-state MOSFET, while the 2nd NDR characteristics is achieved by off-state MOSFET which inhibit the flow of electrons with high channel potential barrier. The front circuit of Fig. 1(a), CMOS STI, is introduced for single input sweep between gate and drain ($V_G$ and $V_D=V_N$), complementary double peak NDR curves of $n/p$NDR, and 5-state latch with the same unit cell area of binary latch circuit. To generate the additional intermediate state of STI based on conventional binary inverter circuit, we used $V_{IN}$ independent junction BTBT currents as dominant off current mechanism with high channel doping concentration (Fig. 1(c)) [5]. When both $n/p$MOS flow the constant off currents with similar trans-conductance, the intermediate state is determined by voltage dividing between $n/p$MOS.

Variable $V_{IN}$ circuit is composed with CMOS STI ($nMOS$ and $pMOS$), n-type NDR ($nNDR$), and p-type NDR ($pNDR$) (b) 2-D cross sectional view and circuit symbol of NDR [4] (c) 2-D cross section view and band-to-band generation view of nMOS for STI [5].
principle where the 1st peak (peak1) and 1st valley (valley1) are generated by a typical tunnel diode behavior and the subsequent 2nd peak (peak2) can be formed by suppressing the 2nd valley (valley2) at the MOSFET off-leakage level. The STI can be suppressed the 2nd valley (valley2) current with complementary $V_G$ for each multiple nNDR ($V_G=0$ V) and pNDR ($V_G=1$ V), whereas PTI or NTI can be applied on only for multiple nNDR or pNDR, respectively. The intermediate state ($V_G=0.5$ V) of STI plays a key role for compact circuit design with 33% area reduction compared with previous work about 5-state latch [4], since it can implement 1st NDR characteristics in both n/pNDR devices by supplying the channel electrons to tunnel diode. Moreover, in terms of bit density, 57% reduced number of bit can be obtained compared with binary logic. Device simulation was performed by using Sentaurus® 3-D TCAD device simulator with our numerical BTBT model in order to describe BTBT mechanism (peak1) in forward bias of tunnel diode [6].

3. Results and discussion

Figure 3(a) and (b) analyze the multiple NDR characteristics according to design parameters such as doping concentration of $pn$ tunnel diode and VTC of STI. Figure 3(a) shows that the peak1 currents ($I_{peak1}$) by BTBT and valley1 currents ($I_{valley1}$) by TAT increase by field enhancement when doping concentration of $pn$ tunnel junction increases from $1x10^{20}$ to $5x10^{20}$ cm$^{-3}$. In Fig. 3(b), high transition voltage from intermediate to low state ($V_{ML}$: $V_{IN}$ with variation of $±100$mV are converged to 5-states. Transient simulation results of the latch circuit. Initial states of $V_{IN}$ with variation of $±100$mV are converged to 5-states.

4. Conclusions

We proposed the novel 5-state latch with only 4 transistors based on CMOS STI and complementary double-peak NDR devices, which facilitates 57% bit density reduction from the binary latch. Multiple NDR characteristics have been investigated with analysis of current component according to the device design parameters and 5-state latch based on multiple NDR characteristics has been successfully demonstrated with circuit simulations.

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References