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Si-based nonvolatile field effect transistor using low temperature process

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Abstract

Organic Ferroelectric, P(VDF-TrFE) films were fabricated directly on water-repellent hydrogen terminated Si substrate. C-V and I_D-V_G characteristics of field effect transistor using this metal-ferroelectric-semiconductor structure clearly show nonvolatile operation due to ferroelectric polarization switching of P(VDF-TrFE) film. This is the first time to demonstrate the non-volatile carrier modulation in Si using P(VDF-TrFE)/Si interface with the operation voltage as low as 5 V.

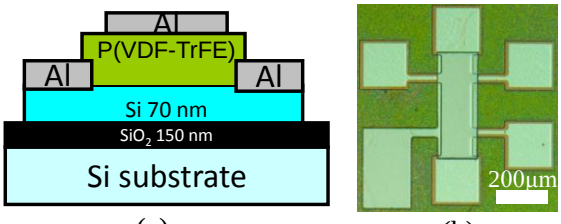
1. Introduction

Ferroelectric-gate field effect transistors (FeFETs) have been extensively studied as non-volatile memory because of its advantages such as good scalability and low power consumption. However, it is quite difficult to get the dielectrically good interface between such ferroelectrics with oxide perovskite structure and the Si substrate due to the formation of low-*k* non-ferroelectric interfacial layer during the deposition of ferroelectric layer, and even at sintering temperature as low as 500 °C [1] that brings about the issues such as an insufficient bias voltage to the ferroelectric layer. As the solution of the problems, a metal-ferroelectric-insulator-semiconductor (MFIS) structure, which has a high-k buffer layer inserted between the ferroelectric and Si layers are reported [2-4]. Although MFIS structure seems to have solved the several problems of the MFS structure, the issue on high voltage operation of FeFETs still exists. On the other hands, organic ferroelectric polar polymers have been exploring as an alternative to inorganic ferroelectrics with higher process temperature because ferroelectric polymers can be deposited on Si at relatively lower temperature as low as 200 °C through solution process [5]. Since Poly-vinylidene fluoride (PVDF) and its copolymers with trifluoroethylene [P(VDF-TrFE)] and tetrafluoroethylene [P(VDF-TeFE)] are the well-known ferroelectric polymers, many studies on the MFIS and MFS structures using these films have been reported [6,7]. In the case of Si based MFS structures using these polymers, however, MFIS structures are usually used because organic ferroelectric films on water-repellent Si surface include numbers of pin-holes [8]. In order to eliminate this problem, thick polymer or inserting thin insulator such as $SiON_x$ or Si_3N_4 is required [7]. Further reducing the operation voltage and increasing ON/OFF ratio while keeping good retention characteristics are still challenging research objects especially for the MFS structures.

In this paper, we demonstrate the fabrication of pin-hole free P(VDF-TrFE) thin films spin-coated directly on water-repellent Si and the non-volatile operation with low voltage.

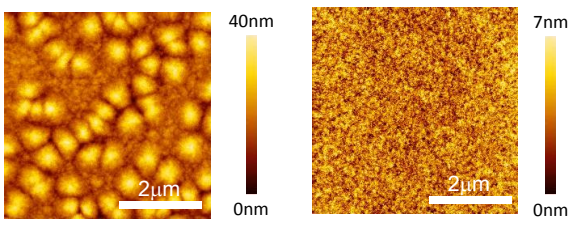
2. Experiment and results

P(VDF-TrFE)(75/25) films were deposited on silicon on insulator (SOI) substrate which consists of Si (70 nm)/ SiO_2 (150 nm)/ Si by spin coating method using a solution of 3 wt.% dissolved in diethyl carbonate. This solution was spin-coated on SOI substrate and annealed at 135 °C for 1h. Then, the samples were slowly cooled from 135 °C to 110 °C at the cooling rate of 10 °C/10 min because the cooling rate across the crystallization temperature mainly affects the crystallinity of P(VDF-TrFE). Al film was deposited on P(VDF-TrFE) by vacuum evaporation and it was patterned by photolithography. Fig. 1 shows the schematic image of the cross sectional view and the optical microscope image of the FET. Before fabrication of P(VDF-TrFE) films, SOI substrate was dipped in 1 % HF solution for 2 minutes in order to remove the natural oxide and formed hydrogen terminated layer. Fig. 2 shows the surface morphologies of P(VDF-TeFE) (a) and P(VDF-TrFE) (b) films deposited on H-terminated Si substrates. Water-repellent of Si and con-



(a) (b)

Fig. 1 Schematic image of cross sectional view, (a), and the optical microscope image, (b), of the FET.



(a) (b)

Fig. 2 Surface morphologies of P(VDF-TeFE) (a) and P(VDF-TrFE) (b) deposited on H terminated Si substrate.

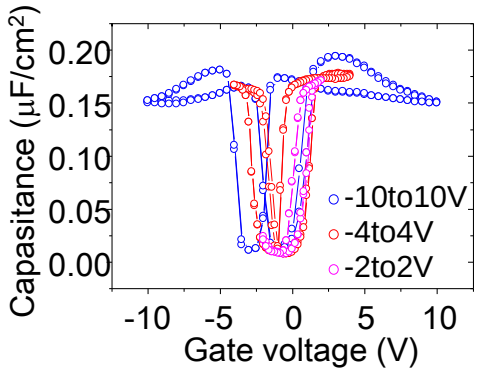


Fig. 3 C-V characteristics of Al/P(VDF-TrFE)/Si MFS structure at the measurement frequency of voltage of 1 kHz.

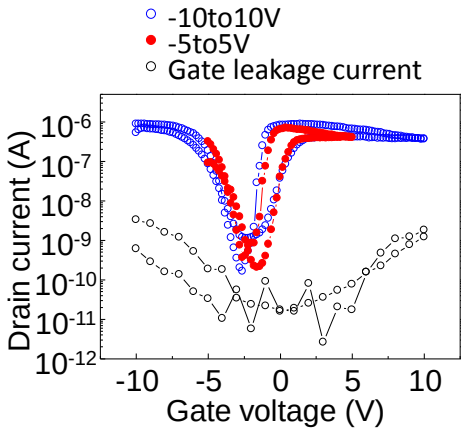


Fig. 4 I_D-V_G and gate leakage current of the FET at the drain voltage of 1 V.

densation of the polymers usually forms non-uniform film as shown in Fig. 2(a). These are the origin of the formation of pin-holes and high leakage current. However, P(VDF-TrFE) film as shown Fig.2 (b) shows relatively uniform surface by optimizing deposition condition such as the atmosphere during deposition, solvent, concentration of solution or annealing sequence. The leakage current of this film is as low as 10^{-8} A even at the applied voltage of 40 V.

Fig. 3 shows C-V characteristics of Si-FET using P(VDF-TrFE) film as gate dielectric. The C-V characteristics show butterfly-like behavior and the capacitance decreases at around zero bias voltage. This behavior should be originated in the carrier modulation in Si suggesting that carrier accumulation occurs at positive bias, depletion at around zero bias and inversion at negative bias. Moreover, the operation voltage is 2 V, which is lower than previous report of MFIS structure [9-11]. In the case of oxide ferroelectrics, the direct contact of a ferroelectric film and semiconductor substrate is difficult to achieve because interdiffusion of constituent elements occurs during the deposition of oxide ferroelectrics. The interdiffusion or SiOx layers usually have much lower dielectric constant than that of ferroelectric films, therefore, it is difficult to apply sufficient voltage to the ferroelectric layer necessary to switch the polarization. However, this C-V characteristics shows clear butterfly hysteric behavior, which means the polarization switching of P(VDF-TrFE) film.

Fig. 4 shows change in the drain current as a function of gate bias V_G. Carrier modulation is clearly observed in this measurement too. The drain current is sufficiently larger than gate leakage current. The ON/OFF ratio and the memory window are calculated as 10^4 and 1 V, respectively. The operation voltage is under 5 V, which is much lower than previous MFIS data as shown in ref. 9-11 keeping that the almost same ON/OFF ratio. This is the first time to demonstrate carrier modulation of Si using Al/P(VDF-TrFE)/Si structure within 5 V.

3. Conclusion

Low voltage carrier modulation of Si using Al/P(VDF-TrFE)/Si structure is demonstrated. C-V characteristics clearly show butterfly-like hysteric behavior suggesting sufficient bias voltage is applied to ferroelectric layer. In spite of almost the same ON/OFF ratio, the operation voltage is as low as 5 V which is much lower than previous reports.

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