Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp122-123

A 16-Level-Cell Memory with 0.24mV/°C Temperature Characteristics comprising Crystalline In–Ga–Zn Oxide FET

Takanori Matsuzaki, Tatsuya Onuki, Shuhei Nagatsuka, Hiroki Inoue, Takahiko Ishizu, Yoshinori Ieda, Naoto Yamade, Hidekazu Miyairi, Masayuki Sakakura, Yutaka Shionoiri, Kiyoshi Kato, Takashi Okuda, Jun Koyama, Yoshitaka Yamamoto and Shunpei Yamazaki

Semiconductor Energy Laboratory Co., Ltd., 398 Hase, Atsugi, Kanagawa, 243-0036, Japan
Phone: +81-46-248-1131 Fax: +81-46-270-3751, E-mail: tm0632@sel.co.jp

Abstract

A 16-level cell is demonstrated using a test chip of nonvolatile oxide semiconductor RAM comprising c-axis aligned crystalline In–Ga–Zn oxide FETs. A V_t cancel write method is employed for dara write. Read voltages are distributed with the maximum 3σ of 37 mV. At temepratures from −40 to 85°C, the voltage distribution range is 0.13 V, and its variation due to varying temperatures is 0.24 mV/°C.

1. Introduction

With recent increase in the number of electronic devices connected to the Internet, the amount of data to be processed is increasing. High-speed and high-density working memory, which has the features of DRAM and NAND flash memory, is required. To satisfy this need, emerging nonvolatile memories such as MRAM and ReRAM have been developed.

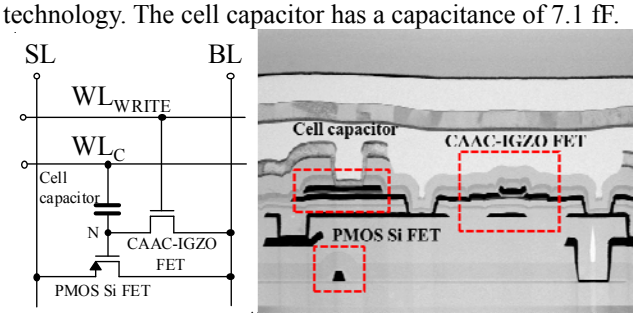
C-axis aligned crystalline In–Ga–Zn oxide (CAAC-IGZO), used in this study, is a crystalline oxide semiconductor and specifically is crystalline IGZO with crystals oriented in the c-axis direction. Using CAAC-IGZO for FET active layers provides an ultralow off-state current of the order of yA/μm (y: 10^{-24}) [1]. The ultralow off-state current enables long-term retention. Nonvolatile oxide semiconductor RAM (NOSRAM) [2] taking advantage of this feature has been proposed.

A NOSRAM cell consists of a CAAC-IGZO FET, a PMOS Si FET, and a cell capacitor. The ultralow off-state current of the CAAC-IGZO FET prevents leakage of charge stored in the capacitor. A conventional NOSRAM cell is limited to an 8-level cell having read voltage distribution with a 3σ of 55 mV [3]. This is because a fluctuation in PMOS threshold voltage due to temperature change increases distribution width; thus, the number of bits per cell cannot be greater than eight.

In this study, with the V_t cancel write method [4], a variation in read voltage distribution caused by a fluctuation in PMOS threshold voltage due to temperature change is reduced, and the voltage distribution is sharpened to achieve 16-level-cell NOSRAM.

2. NOSRAM Cell

Fig. 1(a) is a circuit diagram of a NOSRAM cell. Fig. 1(b) is a cross-sectional micrograph of a NOSRAM cell fabricated with 0.18μm CMOS/0.35μm CAAC-IGZO FET technology. The cell capacitor has a capacitance of 7.1 fF.



(a) (b)

Fig. 1 Circuit diagram and cross-sectional micrograph of a NOSRAM cell.

3. V_t Cancel Write Method

A variation in read voltage distribution due to temperature change is reduced with the V_t cancel write method. First, 0 V is input to BL to turn on the CAAC-IGZO FET, and the voltage V_n of node N is set to 0 V. Then, BL is made floating, and a write voltage V_{write} is input to SL. Thus, the PMOS Si FET is turned on, current flows from SL to BL, and the BL voltage rises. When the CAAC-IGZO FET is on and the BL voltage increases, V_n rises. When V_n reaches $V_{write} - (V_{thp} + \Delta V_{thp})$, the PMOS Si FET is turned off and the BL voltage ceases to rise, resulting in V_n stabilization. Here, V_{thp} is the PMOS Si FET threshold voltage, and ΔV_{thp} is a V_{thp} variation due to temperature change. The CAAC-IGZO FET is then turned off, completing the write operation. After the write operation, the relationship between V_n and V_{thp} is expressed as $V_n = V_{write} - (V_{thp} + \Delta V_{thp})$.

To read data, the SL voltage is lowered by discharging the precharged SL through the PMOS Si FET to BL. As the SL voltage decreases, the gate-source voltage V_{gs} of the PMOS Si FET decreases. When the PMOS V_{gs} reaches close to $V_{thp} + \Delta V_{thp}$, the SL voltage is saturated. The saturation voltage is used as a read voltage V_{read}, where $V_{read} = V_n + (V_{thp} + \Delta V_{thp})$. Here, the SL voltage V_{read} at the time of data reading is $V_{read} = V_{write} - (V_{thp} + \Delta V_{thp}) + (V_{thp} + \Delta V_{thp}) = V_{write}$; i.e., $V_{thp} + \Delta V_{thp}$ is canceled. Thus, a V_{read} distribution variation due to ΔV_{thp} can be reduced.

4. Measurement results and Discussion

Fig. 2 is a die photograph of a fabricated 16-level-cell NOSRAM test chip. The NOSRAM test chip is composed of a NOSRAM cell array, row drivers, 4-bit D/As, input selectors, voltage followers, an output selector, and SL

comparators.

Fig. 3 shows the measured distribution of V_{read} values, which are SL voltages selected during a read operation and are output from the voltage followers. With the V_t cancel write method using CAAC-IGZO FETs, the V_{read} distribution presents a sharp peak with a 3σ of 37 mV (max). This allows separation of 16 distributions without overlap (Fig. 3). Fig. 4 shows 3σ of each data.

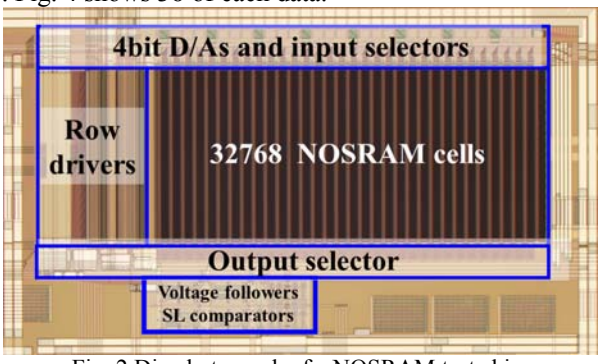


Fig. 2 Die photograph of a NOSRAM test chip.

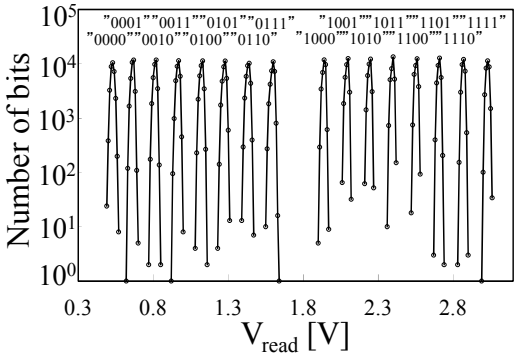


Fig. 3 V_{read} distribution of a NOSRAM test chip.

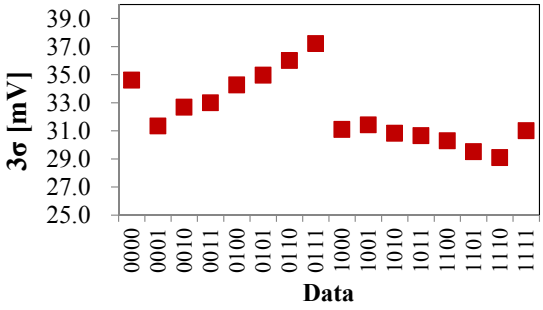
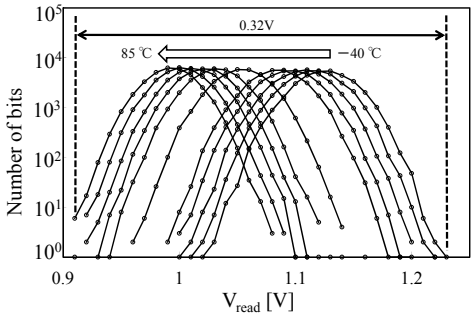


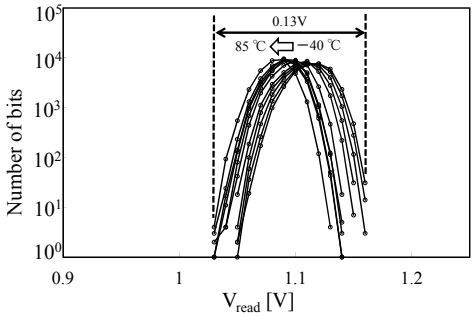
Fig. 4 3σ of each data.

Fig. 5 shows V_{read} distribution at temperatures varying from −40 to 85°C. The distribution range is 0.32 V with a conventional write method (Fig. 5(a)), whereas with the V_t cancel write method, the distribution range is 0.13 V (Fig. 5(b)), which is approximately 59% narrower than the conventional one. A step voltage of V_{write} is 0.17 V, which is larger than the distribution range of 0.13 V. Thus, the V_{read} distributions varied due to temperature change can be separated from each other without overlapping.

Fig. 6 indicates temperature dependence of V_{read} peak. A variation in V_{read} peak due to temperature change is 1.12 mV/°C with the conventional write method and 0.24 mV/°C (reduced by approximately 78%) with the V_t cancel write method. It is demonstrated that the V_t cancel write method reduces variations in NOSRAM cell V_{read} distribution caused by V_{thp} variation due to temperature change.



(a) Conventional write method



(b) V_t cancel write method

Fig. 5 V_{read} distribution at varying temperatures.

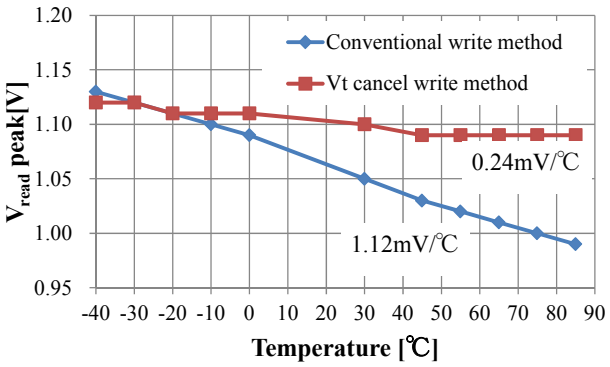


Fig. 6 Temperature dependence of V_{read} peak.

5. Conclusions

A 16-level-cell NOSRAM test chip with CAAC-IGZO FETs is fabricated. With the V_t cancel write method, the V_{read} distribution range is 0.13 V and the V_{read} peak varies by 0.24 mV/°C from −40 to 85°C. The distribution 3σ is 37 mV or less in the 16-level-cell NOSRAM.

The combination of the NOSRAM cell with a CAAC-IGZO FET and the V_t cancel write method achieves a 16-level-cell small-area NOSRAM with little temperature dependence.

References

[1] S. Yamazaki et al., Jpn. J. Appi. Phys., 53, 04ED18 (2014).
[2] H. Inoue *et al.*, IEEE JSSC, 47 (2012) 2258.
[3] S. Nagatsuka *et al.*, *Int. Memory Workshop* (2013) 188.
[4] T. Matsuzaki *et al.*, *ISSCC Dig. Tech. Papers* (2015) 306.