A 16-Level-Cell Memory with 0.24mV/°C Temperature Characteristics comprising Crystalline In–Ga–Zn Oxide FET

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Abstract

A 16-level cell is demonstrated using a test chip of nonvolatile oxide semiconductor RAM comprising C-axis aligned crystalline In–Ga–Zn oxide FETs. A Vt cancel write method is employed for data write. Read voltages are distributed with the maximum 3σ of 37 mV. At temperatures from 40 to 85°C, the voltage distribution range is 0.13 V, and its variation due to varying temperatures is 0.24 mV/°C.

1. Introduction

With recent increase in the number of electronic devices connected to the Internet, the amount of data to be processed is increasing. High-speed and high-density working memory, which has the features of DRAM and NAND flash memory, is required. To satisfy this need, emerging nonvolatile memories such as MRAM and ReRAM have been developed.

C-axis aligned crystalline In–Ga–Zn oxide (CAAC-IGZO), used in this study, is a crystalline oxide semiconductor and specifically is crystalline IGZO with crystals oriented in the c-axis direction. Using CAAC-IGZO for FET active layers provides an ultralow off-state current due to temperature change in PMOS threshold voltage due to temperature change in PMOS off-state current of the order of yA/μm. The ultralow off-state current enables long-term retention. Nonvolatile oxide semiconductor RAM (NOSRAM) [2] taking advantage of this feature has been proposed.

A NOSRAM cell consists of a CAAC-IGZO FET, a PMOS Si FET, and a cell capacitor. The ultralow off-state current of the CAAC-IGZO FET prevents leakage of charge stored in the capacitor. A conventional NOSRAM cell is limited to an 8-level cell having read voltage distribution with a 3σ of 55 mV [3]. This is because a fluctuation in PMOS threshold voltage due to temperature change increases distribution width; thus, the number of bits per cell cannot be greater than eight.

In this study, with the Vt cancel write method [4], a variation in read voltage distribution caused by a fluctuation in PMOS threshold voltage due to temperature change is reduced, and the voltage distribution is sharpened to achieve 16-level-cell NOSRAM.

2. NOSRAM Cell

Fig. 1(a) is a circuit diagram of a NOSRAM cell. Fig. 1(b) is a cross-sectional micrograph of a NOSRAM cell fabricated with 0.18μm CMOS/0.35μm CAAC-IGZO FET technology. The cell capacitor has a capacitance of 7.1 fF.

3. Vt Cancel Write Method

A variation in read voltage distribution due to temperature change is reduced with the Vt cancel write method. First, 0 V is input to BL to turn on the CAAC-IGZO FET, and the voltage Vn of node N is set to 0 V. Then, BL is made floating, and a write voltage V_write is input to SL. Thus, the PMOS Si FET is turned on, current flows from SL to BL, and the BL voltage rises. When the CAAC-IGZO FET is on and the BL voltage increases, Vn rises. When Vn reaches V_write − (Vthp + ΔVthp), the PMOS Si FET is turned off and the BL voltage ceases to rise, resulting in Vn stabilization. Here, Vthp is the PMOS Si FET threshold voltage, and ΔVthp is a Vthp variation due to temperature change. The CAAC-IGZO FET is then turned off, completing the write operation. After the write operation, the relationship between Vn and Vthp is expressed as Vn = V_write − (Vthp + ΔVthp).

To read data, the SL voltage is lowered by discharging the precharged SL through the PMOS Si FET to BL. As the SL voltage decreases, the gate-source voltage Vgs of the PMOS Si FET decreases. When the PMOS Vgs reaches close to Vthp + ΔVthp, the SL voltage is saturated. The saturation voltage is used as a read voltage V_read where V_read = Vn + (Vthp + ΔVthp). Here, the SL voltage V_read at the time of data reading is V_read = V_write − (Vthp + ΔVthp) + Vthp + ΔVthp = V_write, i.e., Vthp + ΔVthp is canceled. Thus, a V_read distribution variation due to ΔVthp can be reduced.

4. Measurement results and Discussion

Fig. 2 is a die photograph of a fabricated 16-level-cell NOSRAM test chip. The NOSRAM test chip is composed of a NOSRAM cell array, row drivers, 4-bit D/As, input selectors, voltage followers, an output selector, and SL...
comparators.

Fig. 3 shows the measured distribution of V_read values, which are SL voltages selected during a read operation and are output from the voltage followers. With the V_t cancel write method using CAAC-IGZO FETs, the V_read distribution presents a sharp peak with a 3σ of 37 mV (max). This allows separation of 16 distributions without overlap (Fig. 3). Fig. 4 shows 3σ of each data.

Fig. 2 Die photograph of a NOSRAM test chip.

Fig. 3 V_read distribution of a NOSRAM test chip.

Fig. 4 3σ of each data.

Fig. 5 shows V_read distribution at varying temperatures from −40 to 85°C. The distribution range is 0.32 V with a conventional write method (Fig. 5(a)), whereas with the V_t cancel write method, the distribution range is 0.13 V (Fig. 5(b)), which is approximately 59% narrower than the conventional one. A step voltage of V_write is 0.17 V, which is larger than the distribution range of 0.13 V. Thus, the V_read distributions varied due to temperature change can be separated from each other without overlapping.

Fig. 6 indicates temperature dependence of V_read peak. A variation in V_read peak due to temperature change is 1.12 mV/°C with the conventional write method and 0.24 mV/°C (reduced by approximately 78%) with the V_t cancel write method. It is demonstrated that the V_t cancel write method reduces variations in NOSRAM cell V_read distribution caused by V_thp variation due to temperature change.

Fig. 5 V_read distribution at varying temperatures.

Fig. 6 Temperature dependence of V_read peak.

5. Conclusions

A 16-level-cell NOSRAM test chip with CAAC-IGZO FETs is fabricated. With the V_t cancel write method, the V_read distribution range is 0.13 V and the V_read peak varies by 0.24 mV/°C from −40 to 85°C. The distribution 3σ is 37 mV or less in the 16-level-cell NOSRAM.

The combination of the NOSRAM cell with a CAAC-IGZO FET and the V_t cancel write method achieves a 16-level-cell small-area NOSRAM with little temperature dependence.

References