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# High-performance In-Ga-Zn-O TFT Memory with Pt nanocrystals

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**Abstract**

**For In-Ga-Zn-O (IGZO) thin-film transistor (TFT) memory devices, how to realize fast electrical erase of the programmed device is still a serious challenge. In this work, the electrical program-erasable IGZO TFT devices with atomic-layer-deposited (ALD) gate stack of $Al_2O_3$/ Pt-nanocrystals/$Al_2O_3$ have been fabricated, exhibiting fast program/erase characteristics. A large memory window of 3.03 V was achieved after +15 V/1 ms programming and -15 V/200 ms erasing. Further, a ten-year memory window of ~2.14V was extrapolated at room temperature. Furthermore, good endurance is also demonstrated.**

## 1. Introduction

An IGZO film has been intensely studied as channel material in TFTs. Further, to develop next-generation system-on-panel displays, IGZO TFT memory has been proposed because it can be easily integrated into displays. However, IGZO is a natural n-type semiconductor, generally supplying only electrons for channel conduction; thus, very few holes are available for device erasure when the gate is negatively biased. This thus results in very poor erase efficiency [1-2]. In this work, the IGZO TFT memory was fabricated using $Al_2O_3$/Pt-nanocrystals/$Al_2O_3$ gate stack, demonstrating fast program/erase characteristics under low voltage, as well as good data retention and endurance.

## 2. Experimental Procedure and Results

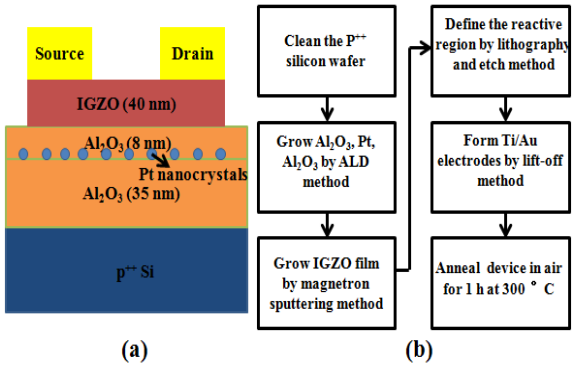


Fig. 1 (a) Schematic cross-sectional view and (b) process flow of the fabricated device.

Fig.1 shows the device structure and fabrication process flow. A 35 nm $Al_2O_3$ film, Pt-nanocrystals and a 8 nm $Al_2O_3$ film were used as the blocking layer, charge storage medium and tunneling layer, respectively. A 40 nm IGZO film was used as channel layer.

Fig. 2(a) shows a cross-sectional TEM image of the fabricated devices. Fig. 2(b) shows SEM image of the ALD Pt nanocrystals with a density as high as ~ $2.17\times10^{12}$ $cm^{-2}$.

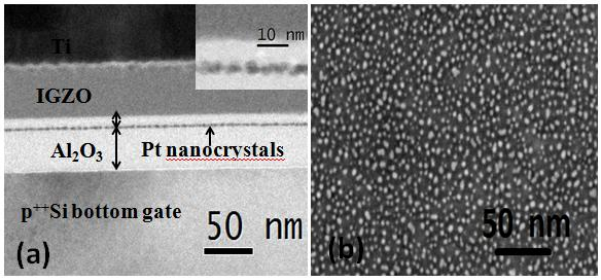


Fig. 2 (a) Cross-sectional TEM image of fabricated memory device and (b) SEM image of Pt nanocrystals.

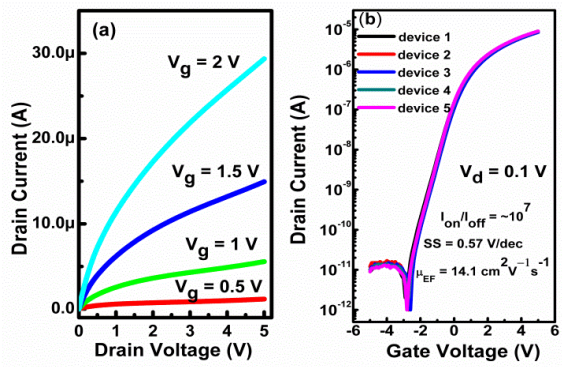


Fig. 3 The output (a) and transfer (b) characteristics of the fabricated TFT devices with Pt-NCs.

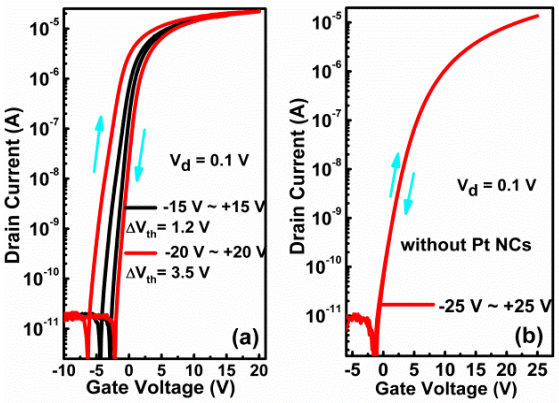


Fig. 4 $I_d$–$V_g$ hysteresis behaviors of the TFT devices: (a) with Pt-nanocrystals; (b) without Pt- nanocrystals.

Fig. 3(a) shows the representative output characteristics of the memory device. Fig. 3(b) shows the transfer characteristics of various memory devices, demonstrating an $I_{on}/I_{off}$ ratio of ~ $10^7$, a sub-threshold swing of 0.57 V/dec, and an effective electron mobility of 14.1 $cm^2/V{\cdot}s$. Meanwhile, it also suggests a good uniformity of the devices.

Fig. 4(a) presents clockwise hysteresis-windows (HWs) of the device with Pt-nanocrystals, revealing an occurrence of remarkable electron trapping in the gate stack. The HW increases from 1.2 to 3.5 V as the gate sweep voltage increases from ± 15 V to ± 20 V. Fig. 4(b) shows a negligible HW for the device without Pt-nanocrystals.

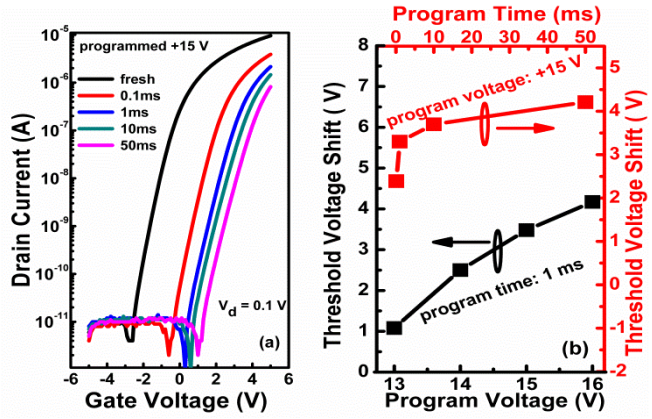


Fig. 5 Programming characteristics of the memory devices as a function of programming time and voltage, respectively.

As shown in Fig. 5, the threshold voltage shift ($\Delta V_{th}$) increases from 2.39 to 4.21 V with increasing the programming time from 0.1 to 50 ms at +15 V. Further, as the programming voltage increases from 13 to 16V, the resulting $\Delta V_{th}$ increases from 1.08 to 4.17 V for a fixed programming time of 1 ms, revealing significant voltage dependence of the program efficiency.

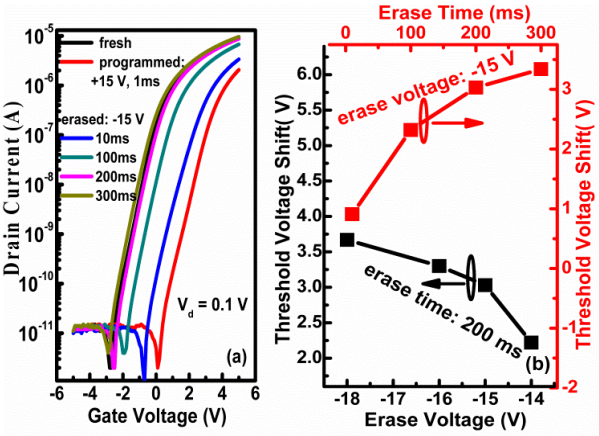


Fig.6 Erase characteristics of the programmed device as a function of erasing time and erasing voltage.

Fig. 6 illustrates the electrical erase characteristics of the programmed device. As the erasing time extends from 10 to 300 ms at -15 V, the $\Delta V_{th}$ increases from 0.91 to 3.34 V. Further, as the erasing voltage increases from -14 to -18 V for a fixed erasing time of 200 ms, $\Delta V_{th}$ increases from 2.22 to 3.67 V. The above results demonstrate a high erase efficiency especially at higher erase voltages, which is related to detrapping of electrons in the Pt nanocrystals.

Fig. 7 shows the data retention characteristics of the memory devices in the programmed/erased states at room temperature. A memory window of ~2.14 V after 10 years is extrapolated after programming at +15V for 1ms and erasing at −15V for 200ms. Furthermore, the memory device also exhibits robust endurance characteristics, as shown in Fig. 8. Both the programmed and erased states are quite stable during $10^3$ cycles of program/erase.

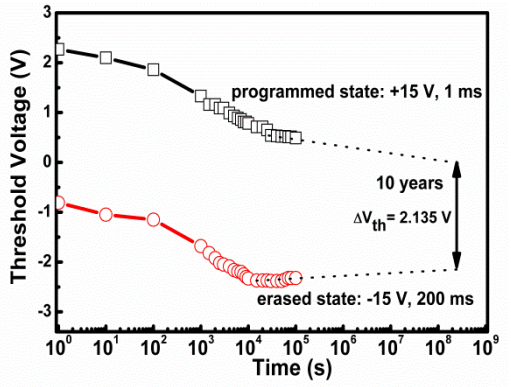


Fig. 7 Data retention characteristics of the memory at RT.

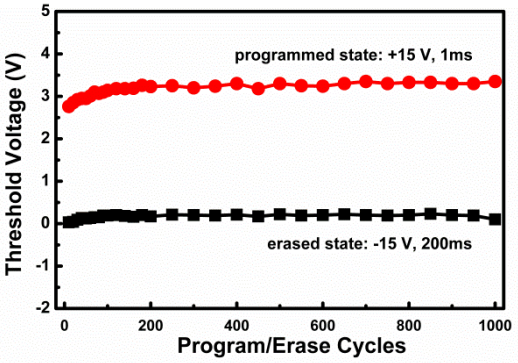


Fig. 8 Endurance characteristics of the memory devices.

## 3. Conclusions

The IGZO TFT memory devices with $Al_2O_3$/Pt-nanocrystals/$Al_2O_3$ exhibit excellent programming and erasing efficiency. A memory window of 2.135 V after 10 years is extrapolated after +15 V/1 ms programming and -15 V/200 ms erasing, and the programmed/erased states are well maintained during $10^3$ cycles of program/erase.

## References


[1] S. Chen, X. M. Cui, S. J. Ding, et al., IEEE Electron Device Lett. **34** (2013) 1008-1010.

[2] H. X. Yin, S. Kim, C. J. Kim, et al., Appl. Phys. Lett. **93** (2008) 172109.