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A Compact 0.3-to-1.125GHz Self-Biased PLL for System-on-Chip Clock Generation in 0.18μm CMOS

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Abstract

A compact ring oscillator based self-biased PLL (SBPLL) for system-on-chip (SoC) clock generation is proposed. It adopts a source degeneration voltage-to-current (V-I) converter and a simple start-up circuit to save the power and area while maintain robust operation. The SBPLL is implemented in 0.18μm CMOS process with an active core area of only 0.048mm^2. It consumes 5.6mW from a 1.6V power supply. The loop bandwidth can be kept around 5MHz at different output frequency. The measured output frequency range is 0.3~1.125GHz and the rms jitter is 2.3ps at output frequency of 1.125GHz.

1. Introduction

Phase-locked loop (PLL) is a critical building block that is widely used in many components of SoC systems. In the design of PLL for SoC clock generation, there are several design challenges such as wide output frequency range, low-jitter performance and insensitivity to PVT variation.

Among most of the PLL architecture, the self-biased PLL (SBPLL) [1] is a good choice to overcome the challenging issues above because the loop bandwidth to reference frequency ratio can be kept relatively constant regardless of output frequency. Thus, a wide loop bandwidth can be set to achieve low-jitter performance. The loop bandwidth is insensitive to the PVT variation.

In this paper, a compact ring oscillator based SBPLL is proposed**.** It adopts a source degeneration voltage-to-current converter (V-I) and a proposed simple start-up circuit to save area and power while maintain robust operation. It occupies only 0.048 mm^2 active area in cheap 0.18μm process, which is a good choice for the clock generation of low-cost SoC application.

2. Architecture of Proposed SBPLL

Fig. 1 shows the block diagram of proposed SBPLL. It consists of a phase/frequency detector (PFD), self-biased charge pump, start-up circuit, source degeneration voltage-to-current (V-I) converter, ring current controlled oscillator (RCCO), frequency divider and output buffer. The reference clock is set to be 75MHz so that a bandwidth as wide as 5MHz can be set to suppress more phase noise from RCCO and thus achieve low-jitter performance.

In this SBPLL, as shown in Fig. 1, the bias current is set proportional to the control current of RCCO to keep loop bandwidth to reference frequency ratio relatively constant. By analyzing the loop dynamics with similar method [1], the loop bandwidth of the proposed SBPLL can be expressed as

$$\omega_{BW} = \frac{A}{2\pi} \times \frac{R_1}{R_2} \times \omega_{REF} \qquad (1)$$

where R_1, R_2 and A are shown in Fig. 1 and ω_{REF} is the angular frequency of the reference clock. Equation (1) indicates that the loop bandwidth to reference clock frequency ratio can not only be kept relatively constant regardless of the divide ratio N but also not sensitive to PVT variation.

Unlike the V-I converter in [1], which is an operational amplifier (OPAMP) based V-I converter, the source degeneration V-I converter is implemented in the proposed SBPLL. The OPAMP is removed in such V-I converter and it consists only 4 MOS transistors and one degeneration resistor, R2. So not only the power and area can be saved but also the phase noise contributed from the OPAMP is eliminated. What's more, the R2 can guarantee the linearity of source degeneration V-I converter not seriously degraded compare to the OPAMP based V-I converter in [1].

In SBPLL, the robust start-up circuit is necessary. Fig. 2(a) shows the schematic of proposed simple start-up circuit. It only includes two PMOS transistors, two switches and one inverter, which occupy negligible area.

The operation process of SBPLL with the proposed start-up circuit is presented in Fig. 2(b), in which the V_C is the control voltage shown in Fig. 1. The operation process include two phase. In the first phase, the reset phase, the SW1, SW2 in start-up circuit is open and SW3 is closed, the loop is open and the V_C is set to be half the supply voltage to make the oscillator and the charge pump start to work. In the second phase, the tracking and locking phase, the reset signal goes high first, then SW2 turns off and SW3 turns on to close the loop and PLL start to lock to the desired frequency. By turning SW1 off, the start-up circuit is turned off not only to save power but also to avoid the affection to the PLL frequency tracking and locking. In summary, the PLL can start up and lock to the desired frequency correctly and robustly by following the process above.

3. Measurement Results

Fig.3 shows the chip microphotograph of the proposed SBPLL. It is implemented with 0.18μm and occupies an active area of only 0.048mm^2 with a 1.6V power supply.

The measurement shows that the SBPLL can generate the clock with frequency range from 300MHz to 1125MHz. The maximum power consumption is 5.6mW at 1125MHz clock output.

The measured phase noise of 10MHz offset frequency is -113dBc/Hz and -115dBc/Hz at clock frequency of 600MHz and 1.125GHz, respectively, as shown in Fig. 4. Such Figure also shows a relatively constant loop bandwidth of 5MHz at different output frequency. Fig. 5 shows the frequency spectrum at 1.125GHz output. The reference spur is -60dB. The performance and summary of the SBPLL is listed in Table I, in which the figure of merit (FOM) is calculated by equation (2) [2].

$$FOM = 10\log[(\frac{\sigma_t}{1s})^2 \times (\frac{P}{1mW})] \qquad (2)$$

4. Conclusions

A compact 0.3GHz-to-1.125GHz SBPLL was proposed and implemented. The power and area can be saved by adopting source degeneration V-I converter and proposed simple start-up circuit. The loop bandwidth can be kept relatively constant regardless of output frequency with the help of self-biased structure. Measurements show this SBPLL has smaller area and lower power than other prior works with comparable FOM.

Acknowledgement

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References

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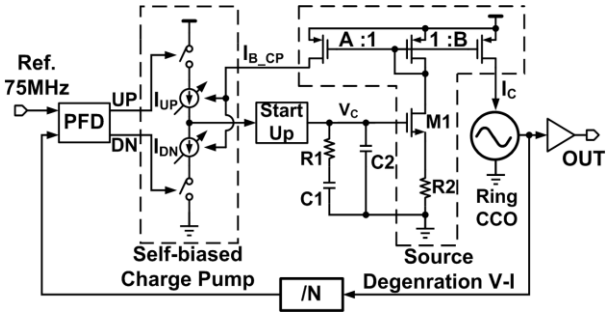
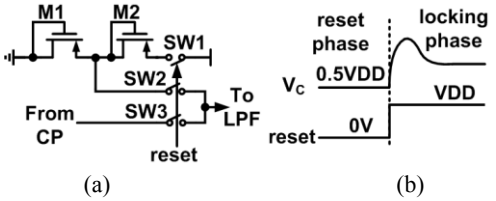


Fig. 1 Block diagram of the proposed SBPLL.



(a) (b)

Fig. 2 (a) Schematic of the proposed start-up circuit. (b) Operation process of proposed SBPLL.

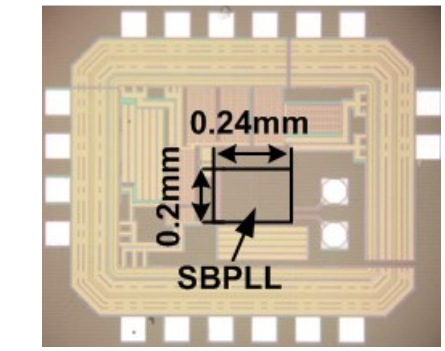


Fig. 3 Chip microphotograph

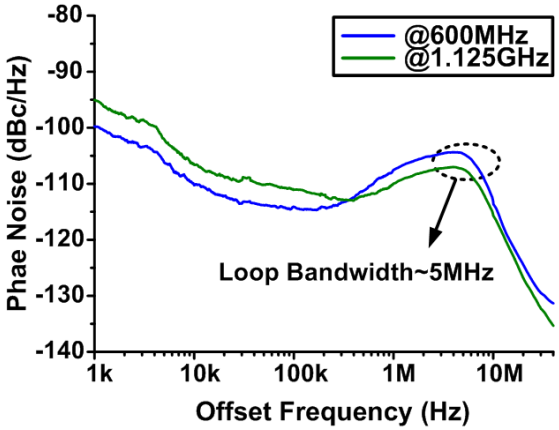


Fig. 4 Phase noise at 1.125GHz and 600MHz, respectively.

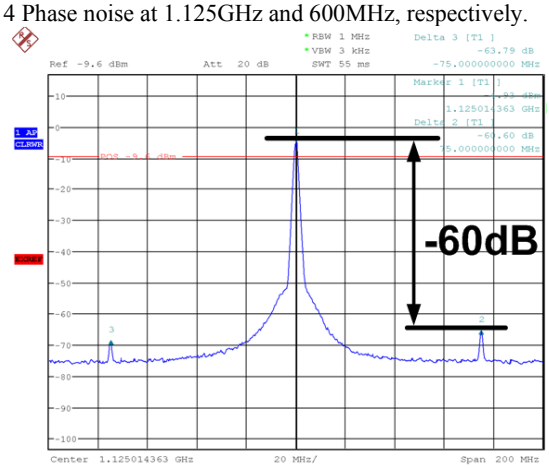


Fig. 5 Frequency spectrum at 1.125GHz

Table I Performance summary and comparison

	This work	ISSCC 2012 [3]	MWCL 2013 [4]	ISSCC 2010 [5]
Output frequency	**0.3~1.125GHz**	3.1 GHz	2GHz	1.21GHz
Phase noise	**-115dBc/Hz @10MHz**	N.A.	-105dBc/Hz @1MHz	-119.6dBc/Hz @1MHz
RMS jitter	**2.3ps (1k~40MHz)**	1.01ps (1k~40MHz)	2.77ps (1k~40MHz)	0.57ps (1k~10MHz)
FOM	**-225.3 dB**	-225.5dB	-216dB	-227.7dB
Reference spur	**-60dB**	N.A.	-50dB	-55dB
Power	**5.6mW**	27.5mW	32mW	51.6mW
Supply Voltage	**1.6V**	1.2V	1.2V	1.2
Area	**0.048mm^2**	0.32 mm^2	0.13 mm^2	0.12 mm^2
Technology	**0.18μm**	65nm	65nm	65nm