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Enhancement Mode AlGaN/GaN MIS-HEMTs Using Multilayer HfO_2/La_2O_3 Gate Insulator for High Power Application

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Abstract

In this study, a gate recessed E-mode AlGaN/GaN MIS-HEMTs using multilayer HfO_2/La_2O_3 gate insulator is presented for high power application. The E-mode device with 10 nm multilayer gate insulator HfO_2/La_2O_3 exhibits maximum current density of 490 mA/mm, maximum transconductance of 140 mS/mm, low subthreshold slope (SS) of 97.8 mV/decade and low threshold voltage hysteresis.

1. Introduction

Recently, AlGaN/GaN high-electron-mobility transistor (HEMT) devices have become very popular for power device application, due to their excellent electric properties, such as wide bandgap (3.4 eV), high saturation velocity (2.5×10^7 cm/s), large breakdown electrical field (3.3 MV/cm) [1]. Because the AlGaN/GaN HEMTs power devices are potential candidates for the electrical vehicle applications, it is necessary to have E-mode AlGaN/GaN HEMTs in view of safety issue and simple design on the circuit [2]. In order to improve performance of E-mode device, we would use gate insulator to get some goals, such as higher gate voltage swing, lower gate leakage current or more positive threshold voltage. However, when the E-mode AlGaN/GaN MIS-HEMTs are used for high power device, the high positive gate voltage may induce the electrons in the 2DEG channel into the deep states at the interface between insulator and AlGaN layer, and results in the threshold voltage hysteresis effect [3].

In this study, we fabricated a gate recessed AlGaN/GaN MIS-HEMT with multilayer HfO_2/La_2O_3 gate insulator. Because oxygen vacancy density in HfLaO is reduced, it is proven to improve V_{th} instability effectively [4]. As a result, we decide to take the composite insulator HfO_2/La_2O_3 as the gate insulator. The device shows low threshold voltage hysteresis with proved capacitance-voltage and DC characteristic.

2. Device fabrication and measurement

The wafers used in this study were grown by MOCVD on the silicon substrate, it includes a 1 µm GaN buffer, a 25 nm undoped AlGaN barrier and 10 nm undoped GaN cap layer. For the device fabrication, first, the multilayer metal of Ti/Al/Ni/Au was deposited by E-Gun evaporator and annealed by rapid thermal annealing (RTA) system at 800 ℃ for 60 seconds in N_2 ambient to form Ohmic contacts. Then, the mesa isolation was formed by using inductively coupled plasma (ICP) etch with Cl_2 gas to define the active region, the etching depth was 200 nm. Then, the multilayer HfO_2/La_2O_3 gate insulator was deposited by molecular beam deposition (MBD) after gate region etching. The gate length was 2 µm. Afterward, a post–deposition annealing (PDA) was carried out at 600 ℃ in N_2 ambient for 5 minutes. Finally, Ni/Au gate metal was deposited by E-Gun evaporator and the gate region was defined by etching (Fig. 1(a)). Furthermore, the MOS capacitor was fabricated to investigate the quality of the HfO_2/La_2O_3 stack gate insulator, as shown in Fig. 1(b).

Agilent E5270B power device analyzer was used for DC characteristic and hysteresis measurement of the samples. Capacitance-voltage characteristic and off-state breakdown voltage of the samples were measured by Agilent 4284 LCR meter and Agilent B1505A power device analyzer, respectively.

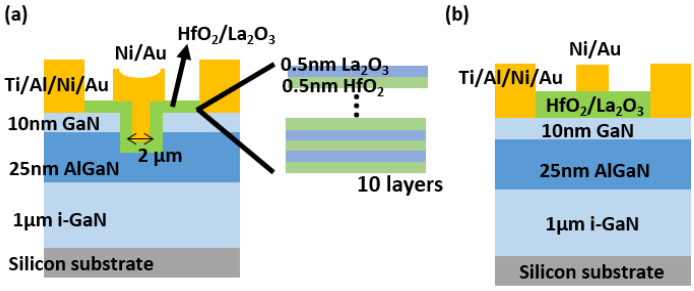

Fig. 1. (a) The structure of the device (b) The structure of the MOS capacitor.

3. Results and discussions

3.1 DC measurements

In Fig. 2(a), the maximum drain-source current of 490 mA/mm at V_{GS} = 4.5 V and V_{DS} = 7 V is observed. Fig. 2(b) shows a threshold voltage of 0.4 V by linear extrapolation of the transfer curve and maximum transconductance of $G_{m,max}$ = 140 mS/mm at V_{GS} = 1.6 V and V_{DS} = 10 V. The subthreshold slope (SS) of the sample is 97.8 mV/decade.

3.2 Breakdown voltage test

The breakdown voltage of the gate recessed MIS-HEMTs with HfO_2/La_2O_3 stack gate insulator is shown in Fig. 3. When the drain bias was increased to 510 V, I_{DS} = 1 mA/mm at V_{GS} = 0 V.

3.3 Hysteresis effect

The possible reason of the threshold voltage shift is due to the traps at the insulator/AlGaN interface which cause the hysteresis effect in the I-V curve. To test the quality of the insulator HfO_2/La_2O_3 of the MOS capacitor was measured the capacitance-voltage characteristic [4]. The results are shown in Fig. 4(a). After the test, the V_{th} hysteresis shows a small shift when the bias swept from -5 V to +2 V and +2 V to -5 V for the E-mode AlGaN/GaN MIS-HEMTs. Therefore, HfO_2/La_2O_3 was used as the stack gate insulator. Fig. 4(b) shows the low hysteresis effect as predicted.

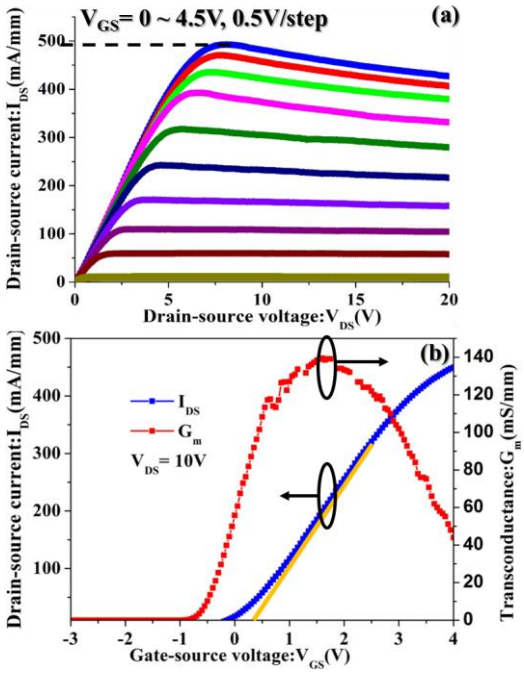

Fig. 2. (a) I_D-V_D characteristics (b) I_D/G_m-V_G characteristics of gate recessed MIS-HEMTs with HfO_2/La_2O_3 stack gate insulator.

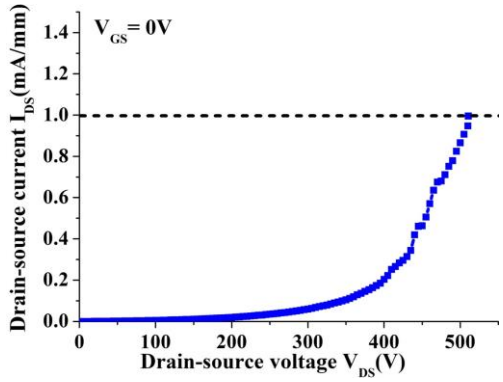

Fig. 3. The off-state breakdown characteristic of gate recessed MIS-HEMTs with HfO_2/La_2O_3 stack gate insulator.

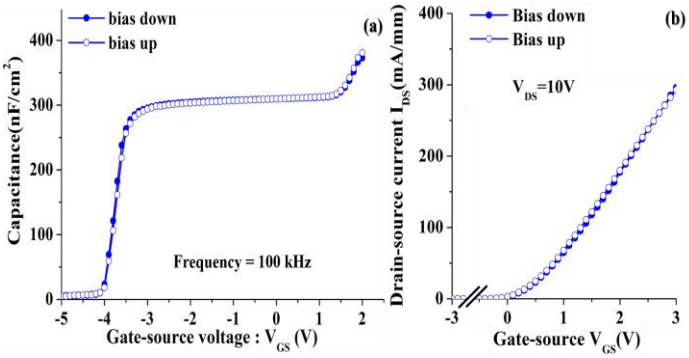

Fig. 4 (a) Hysteresis of capacitance-voltage curve. (b) Hysteresis of I_{DS}-V_{GS} curve of gate recessed MIS-HEMTs with HfO_2/La_2O_3 stack gate insulator.

4. Conclusions

In this study, an E-mode GaN MIS-HEMT with HfO_2/La_2O_3 stack gate is inverstigated. The device showed a positive threshold voltage, a maximum current density of 490 mA/mm, a maximum transconductance of 140 mS/mm and an off-state breakdown of 510 V. Moreover, the device demonstrated a low threshold voltage hysteresis. Compared to the other gate insulator, as shown in Table 1, the composite insulator HfO_2/La_2O_3 is a very promising gate stack insulator for the E-mode AlGaN/GaN MIS-HEMTs for high power application.

Table 1.

Gate insulator	V_{th} / L_g /t_{ox}	I_D / $G_{m,max}$	Breakdown voltage	hysteresis effect
HfO_2 /La_2O_3	0.4 V / 2 µm /10 nm	443 mA/mm (V_{DS}= 10 V V_{GS}= 4 V) /140 mS/mm (V_{DS}= 10 V V_{GS}= 1.6 V)	510 V	45.5 mV
Al_2O_3 [6]	1.7 V / 1.5µm /10 nm	200 mA/mm (V_{DS}= 10 V V_{GS}= 4V) /114 mS/mm (V_{DS}= 10 V V_{GS}= 3 V)	182 V	0.7 V

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