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Selective-Area Growth of Heavily n-Doped c-GaN/GaAs Nanostubs on Si(100) Substrate by Molecular Beam Epitaxy

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Abstract

We successfully demonstrate selective-area epitaxy (SAE) of nearly strain-free defect-free single-crystalline heavily n-doped thin GaAs nanostubs on Si(100) substrates by molecular beam epitaxy (MBE) to utilize them as a buffer layer for subsequent defect-free cubic GaN (c-GaN) nanostub growth. Structural properties and initial nucleation stage control of SAE of n-GaN/n-GaAs are investigated.

1. Introduction

Extensive efforts have recently been put into the development of heterogeneous integration technologies, which enable high performance compound semiconductor devices to be integrated with cost-effective and high density mainstream VLSI CMOS platform [1]. Among those materials systems, a noticeable progress was shown for wide-bandgap GaN devices, thanks to advanced epitaxial techniques [2], [3]. However, it is very challenging to reduce high density of defects formed inside GaN films grown on Si substrates due to their large lattice and thermal mismatches. Although Nanoheteroepitaxy (NHE) is theoretically proven to minimize the defect density in highly mismatched material systems [4]-[6], a mixture of wurtzite and zinc-blende phases in GaN films grown on Si(100) leads to further performance degradation [7]. In this regard, a few research groups have reported planar GaN film growth with mostly zinc-blende phase utilizing GaAs(100) substrates [8], [9], where large defect density still poses a problem. In this study, initial nucleation stage of selective-area growth of heavily n-doped c-GaN nanostubs on n-GaAs/Si(100) by molecular beam epitaxy (MBE) is reported.

2. Results and Discussion

Experimental Details

70nm-thick thermally-grown SiO_2 mask film was patterned utilizing e-beam lithography and CHF_3-based reactive ion etching (RIE). After surface cleaning steps, nanopatterned template was transferred to UHV MBE system. In-situ thermal desorption was performed before growth at high substrate temperature (i.e. >800°C) for native oxide removal on the exposed Si area. Heavily n-doped thin GaAs nanostubs were selectively grown on the exposed Si to be utilized as a buffer layer for subsequent c-GaN growth. The heavily n-doped c-GaN growth was done by selective Ga droplet deposition followed by nitridation of the Ga droplets. Schematic diagram of the above growth procedures is illustrated in Fig. 1.

Selective-Area Growth of n-GaAs Nanostubs

Complete selective-area growth of nearly strain-free single-crystalline diamond-shaped heavily n-doped GaAs nanostubs on Si(100) with excellent film quality was obtained. Structural properties of the GaAs nanostubs were studied using field-emission scanning electron microscopy (FESEM) and high-resolution cross-sectional transmission electron microscopy (HRXTEM). Complete selectivity by MBE with reduced defect density was achieved with four lowest surface energy facets on top shown in Fig. 2(a). In agreement with the literature [5], stacking faults were formed along the preferred {111} plane without the presence of threading dislocations prevalent in planar GaAs film growth on Si(100). These stacking faults were effectively terminated by the nearest sidewalls. More than 70% of the n-GaAs nanostubs are defect-free with less than 0.4% compressive strain parallel to the interface.

Selective-Area Growth of n-GaN Nanostubs

Thin (i.e. < 30nm) heavily n-doped GaAs nanostubs were grown on Si(100) using the optimized growth parameters, to be utilized as a buffer layer for successful demonstration of c-GaN nanostub growth on Si(100). Fig. 3 shows FESEM image of selective-area epitaxy (SAE) of thin n-GaAs nanostub buffer layer. Migration-enhanced epitaxy (MEE) [10] is utilized to achieve smooth morphologies. Due to n-GaAs buffer layer loss during high-temperature GaN growth, Ga droplets are selectively deposited at a substrate temperature of 605°C, capping the underneath thin n-GaAs buffer layer as demonstrated in Fig. 4. These selectively deposited Ga droplets underwent nitridation at different substrate temperatures ranging between 300°C and 600°C to study the initial nucleation stage of its growth. As can be seen from Fig. 5, higher substrate temperature resulted in smoother c-GaN morphologies.

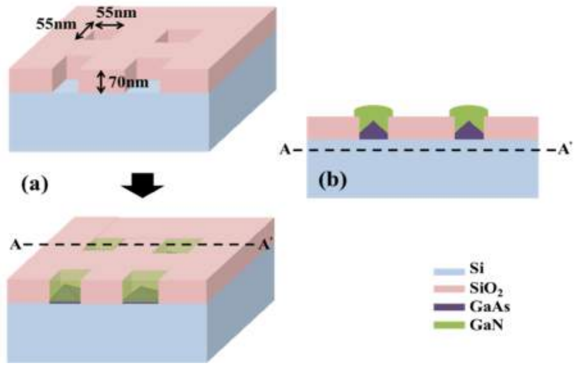

Fig. 1 Schematic diagram of (a) selective-area epitaxy of sub-100nm n-GaN/GaAs nanostubs on Si(100) and (b) cross-section cut along A-A'

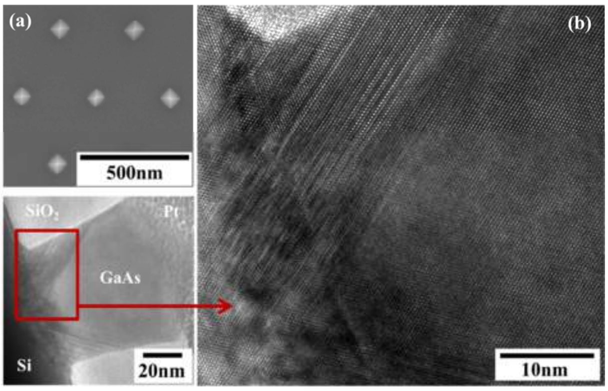

Fig. 2 (a) FESEM and (b) HRXTEM images of 50nm n-GaAs nanostubs on Si(100)

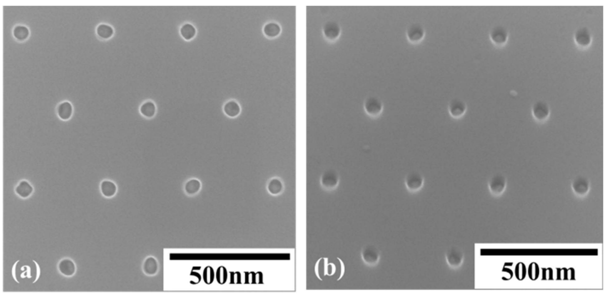

Fig. 3 FESEM (a) plan view and (b) tilted view images of selectively grown sub-100nm n-GaAs nanostub thin buffer layer on SiO_2-patterned Si(100)

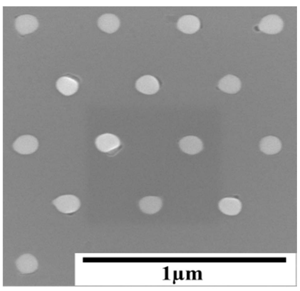

Fig. 4 FESEM image of selective-area Ga droplet deposition on top of as-grown n-GaAs nanostub buffer layer on Si(100)

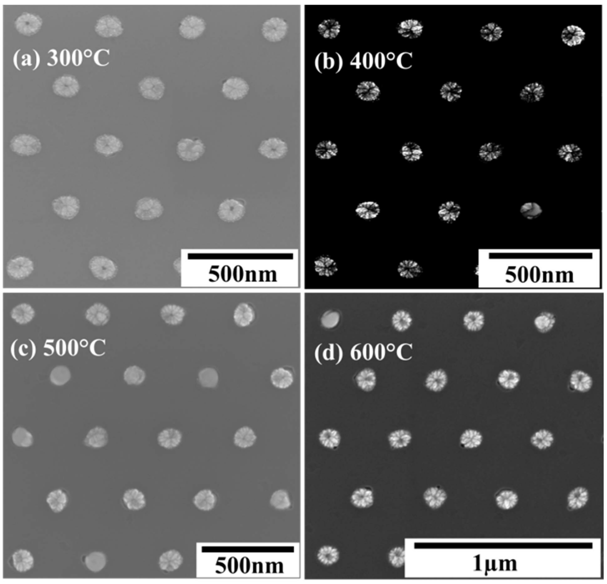

Fig. 5 FESEM images of selectively grown Ga droplet nitridation at (a) 300°C (b) 400°C (c) 500°C and (d) 600°C

3. Conclusions

In conclusion, nearly strain-free, defect-free single-crystalline heavily n-doped thin sub-100nm-diameter GaAs nanostub buffer layer has been successfully demonstrated utilizing MEE. This thin n-GaAs nanostubs serve as a buffer layer to realize selective-area growth of defect-free single-crystalline c-GaN nanostubs on Si(100) substrates. A more detailed structural and electrical characterization on c-GaN nanostubs will be carried out, and the results will be presented at the conference.

Acknowledgements

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