Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp332-333

All oxide all solution-processed active matrix thin-film transistor for electrophoretic display application

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Abstract

Electrophoretic displays (EPD) driven by all oxide thin-film transistors were developed for the first time by using a totally solution process. In TFTs, RuO_2, La-Zr-O (LZO), Zr-In-Zn-O materials were utilized for gate lines, gate insulator, semiconducting channel layers, respectively. The EPDs having the resolution of 101.6 ppi could successfully display the bi-stable patterns.

1. Introduction

In the production of flat panel displays, enlargement of a substrate has been repeatedly conducted to enhance productivity. Now it reached at the size of more than 3 m × 3 m. This trend makes the vacuum deposition apparatus more difficult to be developed and raw material utilization efficiency strictly lower. A sophisticated solution process to replace the conventional vacuum deposition is strongly desired. However, most solution processes ever developed have only focused on a semiconducting channel layer [1]. Here we introduce a total solution process in thin-film transistor (TFT) production, in which all layers of a TFT are fabricated by the solution process. By using it, an electrophoretic display (EPD) was successfully developed.

2. General Instructions

Totally solution process, TFT fabrication and EPD specification

Figure 1(a) shows a plane view of TFT-EPDs with the display area of 6 mm × 6 mm. TFTs with bottom-gate top-contact structure were used for the pixel as shown in the Fig. 1(b). The EPD fabrication process consists of seven photo-masks for particular layer. Table 1 shows the precursor solutions and annealing conditions for each layer in TFT-EPD. RuO_2 is a conductive material and was used for the gate lines and pixel electrodes. LaZrO and ZrInZnO were applied for the gate insulator and channel layer, respectively. Source lines/drain electrodes have the double-layer structure consisting of RuO_2 and ITO. SiO_2 was used for the etch stopper and passivation layers. In the fabrication process, all layers were formed by spin-coating and annealed by rapid thermal annealing system or hot plate. The maximum process temperature was 550 ^oC. Figure 2 (a) and (b) show a diagram of a pixel layout and microscope image of a fabricated pixel TFT, respectively. W and L of the pixel TFTs are 20 and 40 μm, respectively. Number of pixel is 24 × 24 with a pitch of 250 μm × 250 μm, which corresponds to 101.6 ppi resolution. The aperture ratio is 84.6 %. The electrophoretic material consists of microcapsules and binder. Positively charged white pigment particles and negatively charged black ones are suspended into an organic solvent, and this fluid is encapsulated into microcapsules. These microcapsules are blended with a binder, which are coated on plastic films with ITO layers. We fabricated EPDs by laminating EPD sheets on the TFT backplanes. ITO layers of EPD sheets were used for the counter electrode. The TFT-EPD panels and FPCs (Flexible Printed Circuit) were connected by the wire-bonding method; therefore Al-pads were formed on the gate and source line terminals for the connection of Au wire.

TFT characteristics and EPD performance

Figure 3 shows the transfer and output characteristics of the fabricated TFTs. The field-effect mobility, sub-threshold swing, threshold voltage, and "on/off" current ratio were 2.68 $cm^2V^{-1}s^{-1}$, 1.09 V/decade, 3.06 V, and 10^5, respectively. These values are comparable to those obtained by vacuum-processed TFTs [2].

First, the previous displayed images are erased by applying "high" level voltage (V_{DD} = 15 V) to the counter electrode and "low" level voltage (V_{SS} = 0 V) to all pixel electrodes (Erase-mode). Since black pigment particles in microcapsules have the negative charge, all black images are displayed by the Erase-mode operation, which is shown in Fig. 4(a). Then, "low" level voltage is applied to the counter electrode, while an appropriate voltage is applied to each pixel electrode (Write-mode). Figure 4(b) shows a displayed image (check patterns) of TFT-EDPs. It should be noted that the displayed images of EPDs are retained after cutting off the power supply and video signals. This driving sequence and the features of EPDs are suitable for

electronic papers.

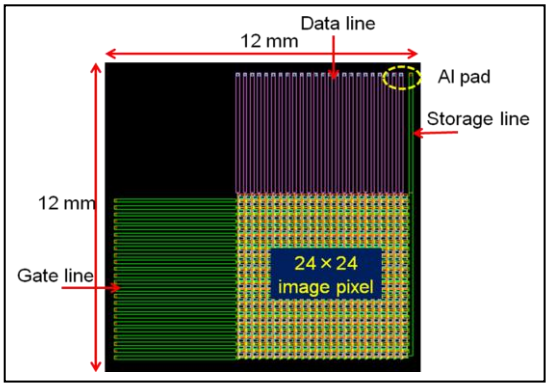

Fig. 1(a). A plane view of TFT-EPDs with the display area of 6 mm × 6 mm.

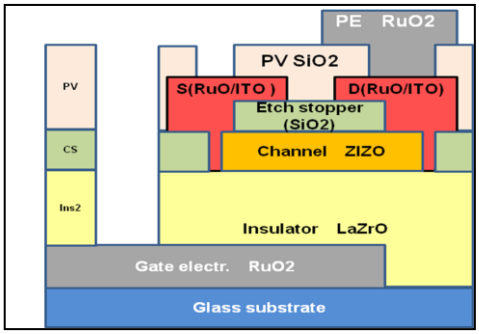

Fig. 1(b). A cross-sectional structure of the pixel TFT.

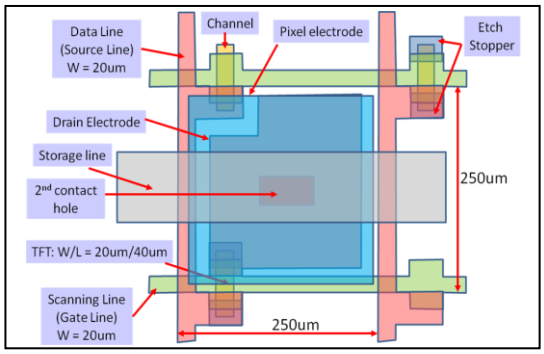

Fig. 2(a). Diagram of the pixel layout in TFT-EPDs.

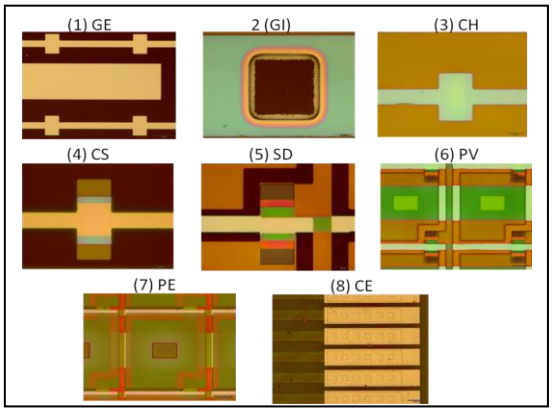

Fig. 2(b). Optical microscope images of each layer in TFT-EPDs.

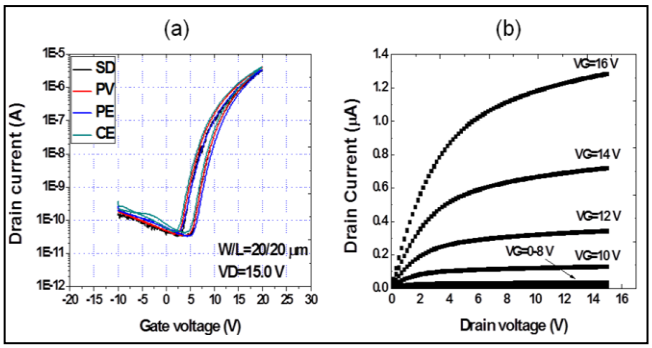

Fig. 3. Transfer (a) and output (b) characteristics of the TFT.

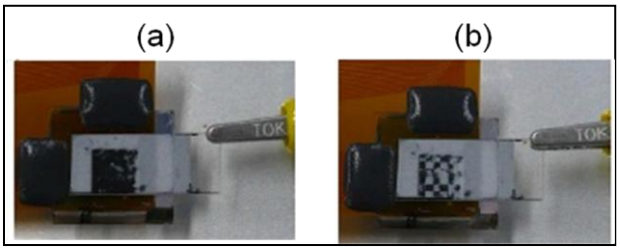

Fig. 4. Display images of TFT-FPDs at: (a) Erase-mode, and (b) Write-mode.

Table I Materials and annealing conditions

Layer	Material	Precursor material	Solvent	T_{anneal} (°C)
Gate line (GE)	RuO_2	$Ru(NO)(NO_3)_3$	PrA, MEA	500
Gate Insulator (GI)	LaZrO	$La(CH_3COO)_3$ $Zr(OC_4H_9)_4$	PrA	550
Channel layer (CH)	ZrInZnO	$Zr(OC_4H_9)_4$ $In(OCCH_3CHOCCH_3)_3$ $ZnCl_2$	PrA 2ME	550
Etch stopper (CS)	SiO_2	Polysilazane		500
Source/ Drain (SD)	RuO_2/ ITO	$Ru(NO)(NO_3)_3$ $In(NO_3)_3$ $SnCl_2$	MEA PrA 2ME	500
Passivation (PV)	SiO_2	Silsesquioxane		500
Pixel electrode (PE)	RuO_2	$Ru(NO)(NO_3)_3$	PrA, MEA	250

3. Conclusions

The all oxide TFT-EPDs by totally solution process were fabricated for the first time. The displayed images were confirmed and could be retained after cutting off the power supply. It is thought that low-cost electronic papers would be realized by using this technology in the future.

Acknowledgements

We would like to express sincere thanks to members of JST-ERATO Shimoda Project and JST-CREST Takamura Project for their supports and discussion.

References

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