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Low Interface Trap Density in $In_{0.53}Ga_{0.47}As$ Metal-Oxide-Semiconductor Capacitors with Molecular Beam Deposited HfO_2/ La_2O_3 High-κ Dielectrics

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Abstract

In this work, we present the improvement of the interfaces between HfO_2 and $In_{0.53}Ga_{0.47}As$ by a thin La_2O_3 layer. Three structures of HfO_2 (6nm), HfO_2(6nm)/ La_2O_3(0.5nm) and HfO_2 (6nm)/ La_2O_3(1nm) were deposited by molecular beam deposition in ultra-high vacuum conditions and annealed at 450°C for device performance comparison. Excellent capacitance-voltage characteristics have been demonstrated along with unpinned Fermi level. Low Dit of 2×10^{11} $cm^{-2}.eV^{-1}$ was achieved near the mid-gap of $In_{0.53}Ga_{0.47}As$.

1. Introduction

Recently, high electron mobility III-V metal-oxide semiconductor field-effect transistors (MOSFETs) have been widely investigated to replace Si-based complementary metal oxide semiconductor (CMOS)[1,2] due to the much higher electron mobility of the $In_XGa_{1-X}As$ devices. Unlike SiO_2 on Si substrates, the lack of high-quality thermodynamically stable gate dielectric insulators on III–V compound semiconductors remains to be the main challenge to commercialize the III-V MOSFET.

Among various high-k oxides, Al_2O_3, HfO_2 and La_2O_3 have attracted great attention as gate dielectric for InGaAs MOS devices. Al_2O_3 possess high bandgap and good thermal stability while HfO_2 and La_2O_3 has high dielectric constant, which is suitable for further equivalent-oxide-thickness (EOT) scaling. Therefore, interfaces between these high-κ materials and $In_{0.53}Ga_{0.47}As$ have been widely investigated [3-5]. Furthermore, a new high-κ composite structure composed of La_2O_3 and HfO_2 deposited by molecular beam deposition (MBD) showed excellent interface quality and promoted equivalent oxide thickness (EOT) scaling [6,7]. In this study, a thin La_2O_3 passivation layer on $In_{0.53}Ga_{0.47}As$ surface was studied to attain high-quality interface.

2. Device fabrication and measurement

The $In_{0.53}Ga_{0.47}As$ epitaxial layer of the III-V MOS capacitors was grown on the InP substrates. The wafers were first cleaned in 4% HCl solution for 3 minutes. Then, the wafers were loaded into an in situ MBD system to deposit HfO_2(6nm), HfO_2(6nm)/La_2O_3(0.5nm) and HfO_2(6nm) /La_2O_3(1nm) three oxide structures on n-$In_{0.53}Ga_{0.47}As$ at 300°C with an overall pressure of 8×10^{-8} Torr , and the films were annealed in nitrogen gas at 450 °C for 5 minutes. Next, Ni/Au was deposited by electron beam evaporator as gate contact metal. Au/Ge/Ni/Au was deposited by electron beam evaporator on backside of n^+-InP substrate and annealed at 250 ^{0}C for 30 sec for Ohmic contact formation, as shown in Figure 1. The HfO_2/InGaAs without and with 0.5 nm La_2O_3 and 1nm La_2O_3 metal-oxide semiconductor (MOS) capacitors were fabricated and compared.

The capacitance-voltage characteristic was measure by Agilent 4284 LCR meter, and interface trap density was measured by conductance method.

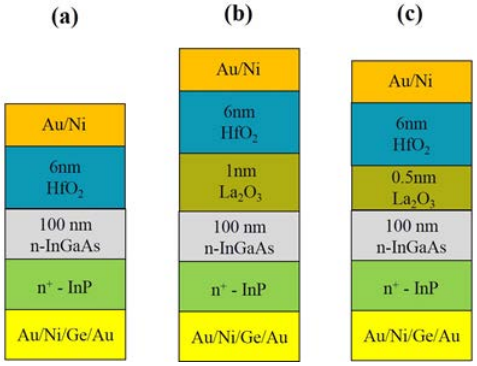

Fig. 1 Schematic illustration of fabricated (a) HfO_2(6nm) (b) HfO_2(6nm)/La_2O_3(1nm) (c) HfO_2(6nm) /La_2O_3(0.5nm) MOS capacitors

3. Results and discussions

Figure 2(a)-(c) shows the multi-frequency C–V curves at low temperature (77K) of the HfO_2/$In_{0.53}Ga_{0.47}As$ MOS capacitor with and without La_2O_3 insertion layer for the devices PDA at 450^{0}C. All of them show good accumulation, depletion and inversion behaviors at room temperature (not shown). After inserting a 1 nm La_2O_3 layer between

the interfaces of $HfO_2/In_{0.53}Ga_{0.47}As$, accumulation capacitance value is degraded. The major cause of this phenomenon is that La_2O_3 reacts with InGaAs substrates to form an intermixed interface layer [8] after PDA at 450°C, forming a interfacial layer which possesses a lower dielectric constant, thus degrade the capacitance value. However, the MOS capacitor with 0.5 nm La_2O_3 insertion layer has higher capacitance value than the 1nm one due to a thinner interfacial layer is formed, because fewer In, Ga and As atoms diffuse into the 0.5 nm La_2O_3 insertion layer.

As presented in Figure 2(a)-(c), the bumps observed at 77K, which attributes to carriers exchange between half of the band-gap located traps and both minority and majority carriers bands[9], indicate that both 1nm and 0.5nm La_2O_3 insertion layer can reduce D_{it} of HfO_2 and $In_{0.53}Ga_{0.47}As$ interface. Figure 2(d) shows the normalized conductance contour as a function gate voltage and frequency (1 kHz–1 MHz) of the HfO_2(6nm) /La_2O_3(0.5nm) MOS capacitor at 77 K. From the figure, the conductance peak maximum can shift along with gate bias and frequency (solid line), indicating that the Fermi level is unpinned.

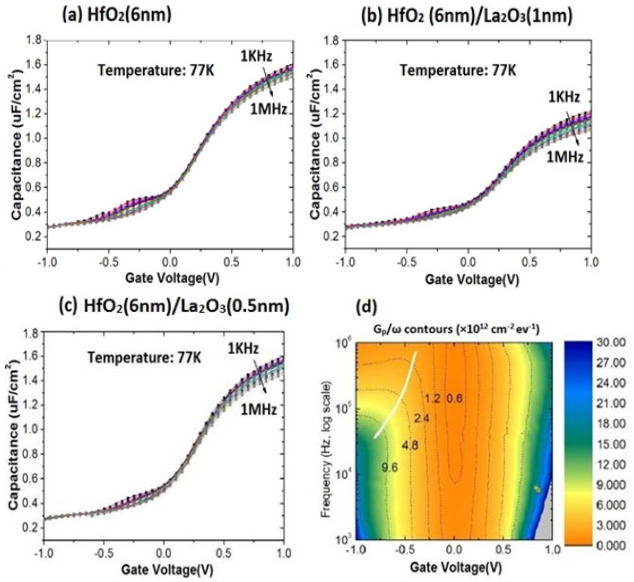

Fig. 2. Multi frequency C-V curve at 77K of the (a) HfO_2(6nm) (b) HfO_2(6nm)/La_2O_3(1nm) (c) HfO_2(6nm) /La_2O_3(0.5nm) MOS capacitors after PDA at 450^0C in N_2 for 5 minutes and (d) Normalized parallel conductance contour map for the HfO_2(6nm) /La_2O_3(0.5nm) MOS capacitor

The Dit distribution as a function of trap energy levels of the samples at 77K is shown in Fig 3. From the figure, excellent Dit of 2×10^{11}–2.4×10^{11} $eV^{-1}cm^2$ in the energy range of 0.37–0.47 eV above $In_{0.53}Ga_{0.47}As$ valence band maximum has been obtained. The great D_{it} of HfO_2(6nm)/ $In_{0.53}Ga_{0.47}As$ MOS capacitor was also achieved as a result of ultra-high vacuum depositing environment of the MBD system. Comparison of Dit and capacitance -quivalent-thickness (CET) with other high-κ materials was shown in Table I.

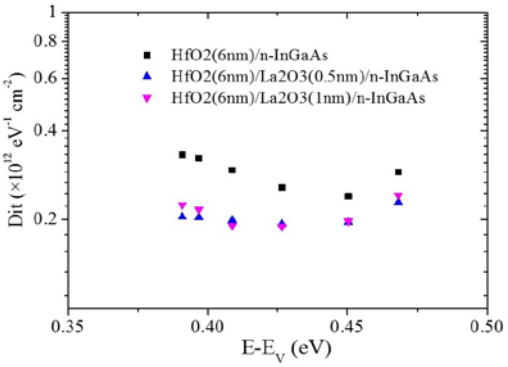

Fig. 3 Interface trap density distribution of the sample extracted by conduction method at 77K.

Table I Comparison of Dit and capacitance -quivalent-thickness (CET) with other high-κ materials on $In_{0.53}Ga_{0.47}As$.

Oxide	Equipment	Dit measurement method	Dit ($10^{12}cm^2$ eV^{-1})	CET@ 1kHz (nm)
HfO_2 (6nm)/ La_2O_3 (0.5nm)	MBD	Conductance	0.2	1.8 @1V
HfO_2 (5.3nm)/ Al_2O_3(1.2nm)[10]	MBD	QS-CV	0.15	1.9 @ 2V
HfO_2(7.8nm) [11]	ALD	Terman	2	1.9 @ 3V
Al_2O_3(5.5nm)[12]	ALD	Conductance	1.7	2.6 @ 3V

4. Conclusions

The HfO_2(6nm), HfO_2(6nm)/La_2O_3(0.5nm) and HfO_2(6nm)/La_2O_3(1nm) on n-$In_{0.53}Ga_{0.47}As$ for MOS capacitor application is investigated. Excellent D_{it} of 2×10^{11} was achieved by inserting a 0.5nm thin La_2O_3 layer between $HfO_2/In_{0.53}Ga_{0.47}As$ interfaces with PDA of 450^0C for 5 minutes. Using a thin La_2O_3 as a passivation layer shows excellent D_{it} while keeping high capacitance value.

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