

# **n<sup>+</sup>Si/pGe Cross Heterojunctions Fabricated by Narrow Membrane Bonding**

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## **Abstract**

n<sup>+</sup>Si/pGe cross heterojunctions were fabricated by narrow membrane bonding with interfaces passivated by amorphous interlayer insertion for the first time. The turn-on voltage was around 0.3V indicating no significant charges induced by the bonded interfaces. The ideality factor of the diode was 1.2 indicating a well passivated interface. This narrow membrane bonding technology shows great potential for bulk material heterojunction formation, especially in cases that ultimately abrupt doping profiles are highly needed.

## **1. Introduction**

Abrupt Si/Ge heterojunctions are highly demanded to ultimately control junction properties as for TFETs and Esaki diodes [1]. Using Conventional epitaxy, they are hard to be formed because of the high temperature process and 4.2% lattice mismatch [2]. Instead of epitaxy, in the direct bonding of semiconductor materials [3]-[7], doping of materials could be done separately leading to ultimately abrupt junctions if the bonding process is conducted at low temperature. However, covalent materials bonding is usually believed to fail since the surface of bulk materials is in principle imperfect. In this paper, bonded rectifying n<sup>+</sup>Si/pGe cross heterojunctions using thermal release tapes to transfer ultra-thin narrow membranes are reported. The interfaces of bonded junctions are well passivated by amorphous interlayer insertion. An ideal turn-on voltage of 0.3V and a much improved diode ideality factor of 1.2 are demonstrated, suggesting great potential for devices utilizing junctions bonded by different bulk materials.

## **2. Experimental Details**

Fig. 1 illustrates schematically how the bonded n<sup>+</sup>Si/pGe heterojunctions were made. The starting materials were a PSG doped n-type ( $1 \times 10^{18} \text{ cm}^{-3}$ ) SOI wafer with a ~70-nm-thick Si layer and a p-type ( $1 \times 10^{16} \text{ cm}^{-3}$ ) GeOI wafer with a ~60-nm-thick Ge layer. 2.6 μm Si and 3 μm Ge wires were made using standard photolithography with H<sub>2</sub>O<sub>2</sub> and NH<sub>3</sub> for etching Ge and TMAH for etching Si, respectively. The patterned SOI wafer was then immersed into 5% HF solution for 2.5 hours to etch away the buried oxide (BOX) layer, leaving only Si wires directly on Si substrate. Then, Si wires were picked up from Si substrate onto the thermal release tape manually. After cleaning and alignment the tape with Si wires was put onto the patterned GeOI wafer and the tape-Si wires-patterned GeOI system was put onto a hot plate at 150°C for 3s. Then Si wires were released from the tape onto the patterned GeOI substrate. Then, samples were annealed in O<sub>2</sub> at 400°C for 30s for forming about 1 nm SiO<sub>2</sub> as the mask for subsequent processes. The passivating interlayer between Si and Ge wires may be formed in the above two processes. Si/Ge crosses were formed by photolithography. Oxide layers were removed for regions where electrodes would be formed by photolithography and 5% HF. Al electrodes was formed followed by annealing in N<sub>2</sub> at 400°C for 30min.

## **3. Results and Discussion**

Images of the bonded junctions with 2.6 μm x 3 μm by an optical microscope and SEM are shown in Fig. 2 demonstrating the bonded junction arrays with flexible ultra-thin narrow membranes. Fig. 3 clearly shows the 3-D image by AFM. Fig. 4 shows the X-TEM images, in which a uniform amorphous interlayer with the thickness of 3.3nm between crystalline Si and Ge is clearly observed. Also note that both Si and Ge show clear lattice images just at the interface. This amorphous interlayer is considered to be a Si oxide layer from the contrast comparison between the interlayer and BOX SiO<sub>2</sub>. When the wires were bonded in the ambient air, the oxygen trapped between the two bonded wires helped to form the amorphous oxide interlayer [8]. Although this interlayer was formed unintentionally during the bonding process, it should help to passivate interface defects to make the diode work, as discussed below.

Fig. 5 shows I-V characteristics of a typical bonded n<sup>+</sup>Si/pGe heterojunction. The turn-on voltage is around 0.3V, almost the same as that in Ge homojunctions. The ideality factor is around 1.2, much improved compared with the wafer bonding case (2.28) [7], indicating a well passivated interface thanks to the interlayer. When the forward bias is increased, the current is limited by the parasitic resistances in series. Despite the good ideality factor, the leakage is large, leading to an on-to-off ratio of ~10<sup>2</sup> at ±2V. This is similar to the wafer bonding case. These phenomenon will be studied through compact modeling.

Fig. 6 shows a possible band diagram and current conduction mechanisms of the bonded n<sup>+</sup>Si/pGe junction. The diffusion current in the neutral regions and the recombination/generation process in the charge space region are considered. The series resistances are also considered. The effects induced by the interlayer are taken into account as follows. First, there may be still traps on the bonded surfaces of Si and Ge, thus the recombination/generation current at the bonded surfaces of Si and Ge is assumed. Second, traps may be formed inside the inserted interlayer. Therefore, the trap-limited mechanism is applied to the carrier transport in the amorphous interlayer. That is, carriers will jump from one trap to another by surmounting the potential barrier [9].

Fig. 5 shows that the proposed model fits well with the data, and several conclusions are 1) The difference between Si and Ge bandgaps leads to a much higher barrier for the diffusion of holes. Therefore the on-current behaves like a n<sup>+</sup>p Ge junction and hole carriers is ignorable, and the turn-on voltage is almost the same as that in Ge (0.3V). This fact suggests no significant charges induced by bonding. 2) When a forward bias is applied, a quite normal recombination process happens in the space charge region and at the bonded surfaces of Si and Ge. Although the surface recombination at the bonded surfaces should be responsible for the nonideal ideality factor (1.2) at the forward bias, it also indicates a good passivation by the interlayer. 3) In a reverse bias case, a much severer generation

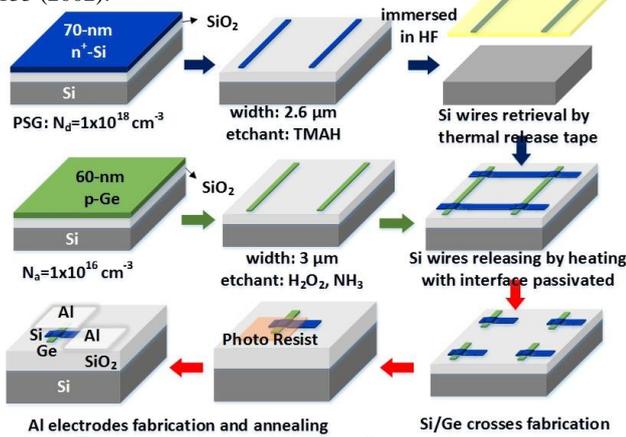
process in the space charge region must be included for describing the large leakage current which increases with the reverse bias in a square root function way. The intense difference between the forward recombination and the reverse generation processes suggests that the current path should be quite different for the two cases. In fact, the junction is bonded in a cross way without sufficient edge or corner passivation. Thus a large generation may happen at the edges and corners in the reversed bias condition [10], while the current may not flow through these places in the forward case. 4) In the interlayer, carriers will jump from a trap around one atom to the trap around a neighboring atom by surmounting 0.327V potential barrier. These high density of traps inside the amorphous interlayer ensure the current conduction through the junction. But the resistance of the interlayer at the forward bias is about 10 times bigger than the wire resistance, thus the amorphous interlayer passivate the interface at the cost of inducing series resistance.

#### 4. Conclusion

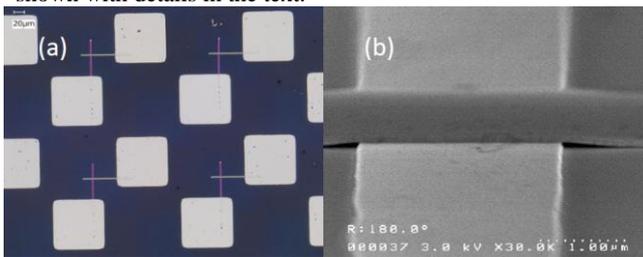
Rectifying n<sup>+</sup>Si/pGe heterojunctions fabricated by ultra-thin narrow membrane bonding have been demonstrated for the first time. The turn-on voltage of 0.3V indicates no significant charges induced by the bonded interfaces. The ideality factor of 1.2 indicates a well passivated interface. The bonded Si/Ge heterojunction with a good ideality factor and an abrupt dopant profile is viable and promising.

#### References

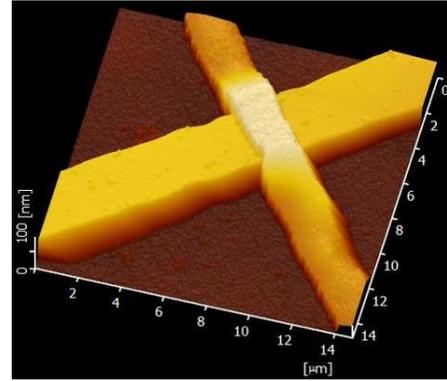
[1] A. Ionescu *et al.*, *Nature*, **479**, 329 (2011). [2] J. Michel *et al.*, *Nature Photonics*, **4**, 527 (2010). [3] S. Chuang *et al.*, *Appl. Phys. Lett.*, **102**, 242101 (2013). [4] T. Roy *et al.*, *ACS Nano*, **8**, 6259 (2014). [5] K. Park *et al.*, *Nano Lett.*, **15**, 289 (2015). [6] A. Kiefer *et al.*, *ACS Nano*, **5**, 1179 (2011). [7] F. Gity *et al.*, *Appl. Phys. Lett.*, **100**, 092102 (2012). [8] J. Rouviere *et al.*, *Appl. Phys. Lett.*, **77**, 1135 (2000). [9] D. Lelmini, *et al.*, *J. Appl. Phys.*, **102**, 054517 (2007). [10] V. Obreja, *IEEE Trans. Electron Dev.*, **49**, 155 (2002).



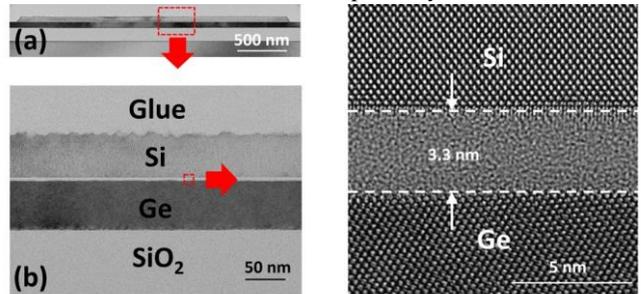
**Fig. 1** Fabrication method of n<sup>+</sup>Si/pGe junctions is schematically shown with details in the text.



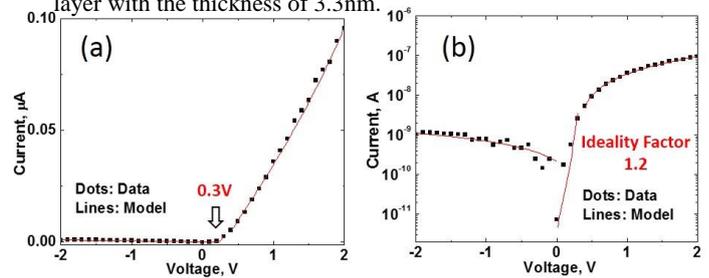
**Fig. 2** Images of the bonded junctions by (a) an optical microscope, and (b) scanning electron microscope (SEM).



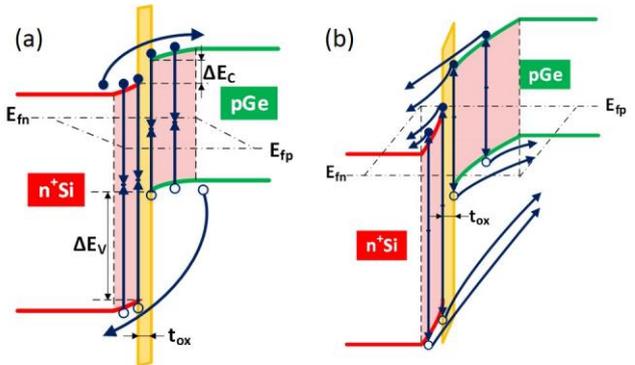
**Fig. 3** AFM results of a bonded Si/Ge heterojunction showing the 3-D structure. RMS roughness for the bonded surfaces of Si and Ge wires is 0.15 nm and 0.18nm respectively.



**Fig. 4** Cross-sectional TEM images of a bonded junction. (a) A TEM image. (b) A magnified TEM image clearly shows a uniform interlayer between Si and Ge wires. (c) A HRTEM image clearly shows both bonded Si and Ge wires remain single crystalline inside the wires while the interlayer is a uniform amorphous layer with the thickness of 3.3nm.



**Fig. 5** I-V characteristics of a typical bonded n<sup>+</sup>Si/pGe heterojunction in the (a) linear scale and (b) semi-log scale. The turn-on voltage and the ideality factor are around 0.3V and 1.2, respectively. Verification of proposed compact models are also shown.



**Fig. 6** Schematic representation of the n<sup>+</sup>Si/pGe band diagram in the present PN junction, illustrating carrier transport mechanisms (a) in the forward bias, and (b) in the reverse bias regions. Trap limited conduction mechanism is applied to the interface layer which will also cause generation and recombination at its surfaces.